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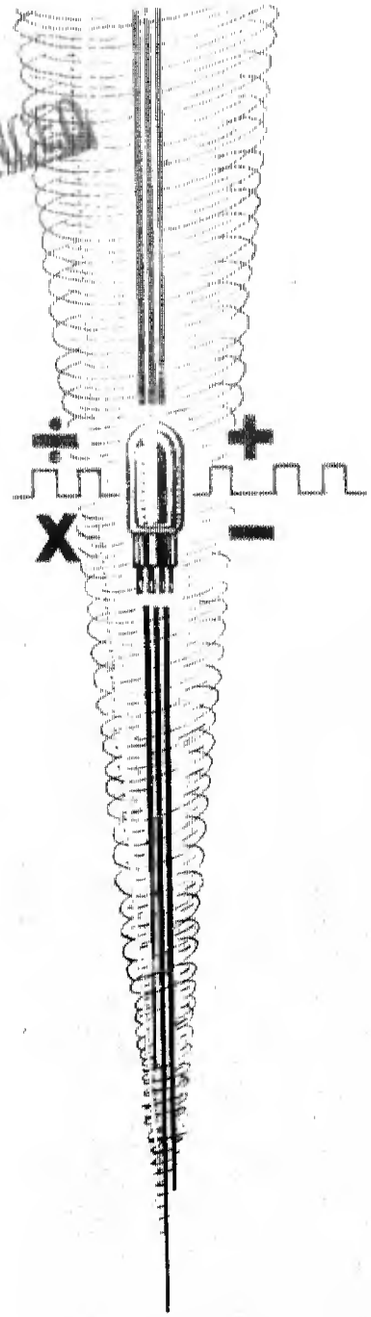


PROJECT
WHIRLWIND

Contract N5ori60

SUMMARY REPORT NO. 2
VOLUME 6

REPORT R-127

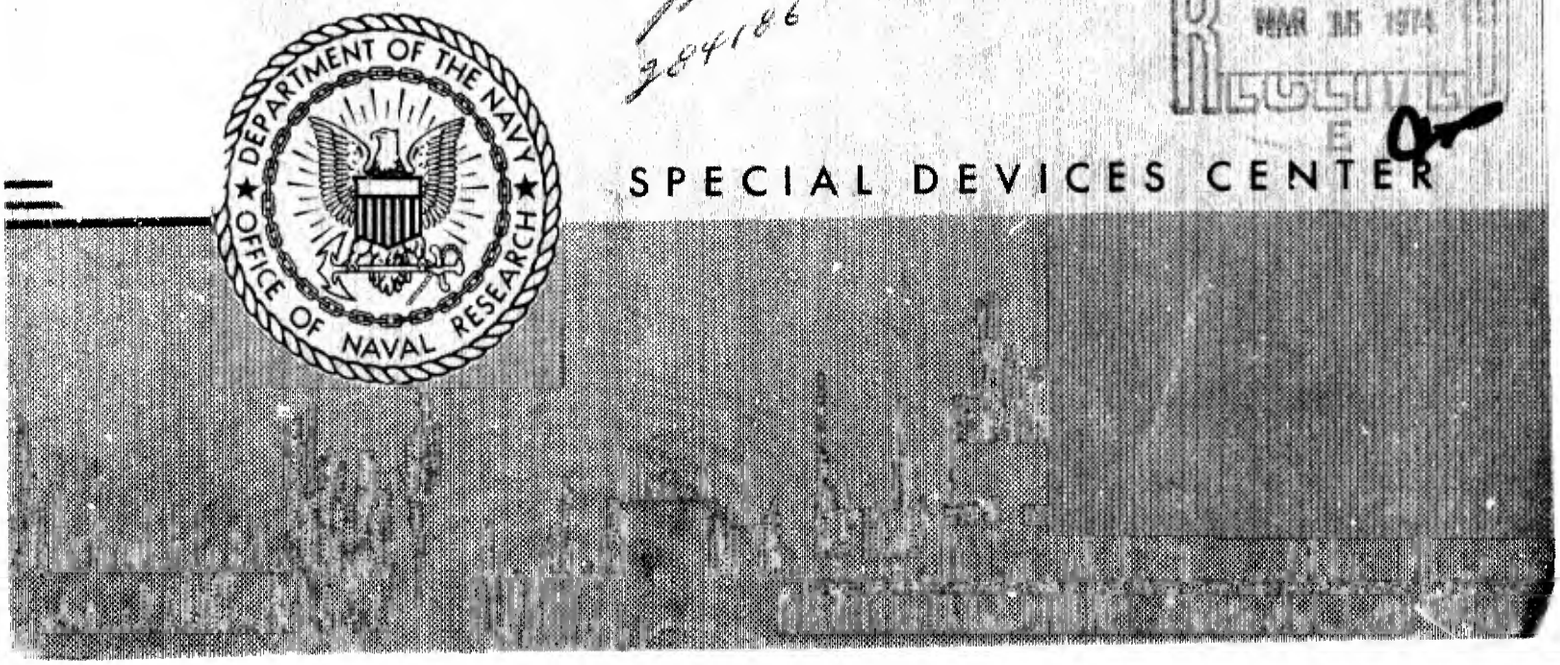
WHIRLWIND I COMPUTER BLOCK DIAGRAMS

VOLUME 2 OF 2 VOLUMES

SERVOMECHANISMS LABORATORY
MASSACHUSETTS INSTITUTE OF TECHNOLOGY

September 4, 1947

SPECIAL DEVICES CENTER



PROJECT WHIRLWIND.

(DEVICE 24-X-3)

REPORT R-127

WHIRLWIND I COMPUTER BLOCK DIAGRAMS,

VOLUME 2 OF 2 VOLUMES

Submitted to the

SPECIAL DEVICES CENTER

OFFICE OF NAVAL RESEARCH

Under Contract N5ori60

Report by

R. R. Everett & F. E. Swain

SERVOMECHANISMS LABORATORY

MASSACHUSETTS INSTITUTE OF TECHNOLOGY

Cambridge 39, Massachusetts

MIT-
Project DIC-6345

September 4, 1947

78 p.

FOREWORD

This report is a description of the Whirlwind electronic digital computers under development at the Servomechanisms Laboratory of M. I. T. for the Office of Naval Research. The arithmetic nature and the physical nature of the computers are covered briefly, and the block diagrams for the prototype computer WWI are discussed in some detail.

The report consists of two volumes: Volume 1 contains the text and Volume 2 the drawings.

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LIST OF DRAWINGS

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54	C–37077	Operation Matrix I
55	C–37078	Operation Matrix II
56	B–37076	Time Pulse Distributor Control
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59	C–37064	Storage Chassis Arrangement
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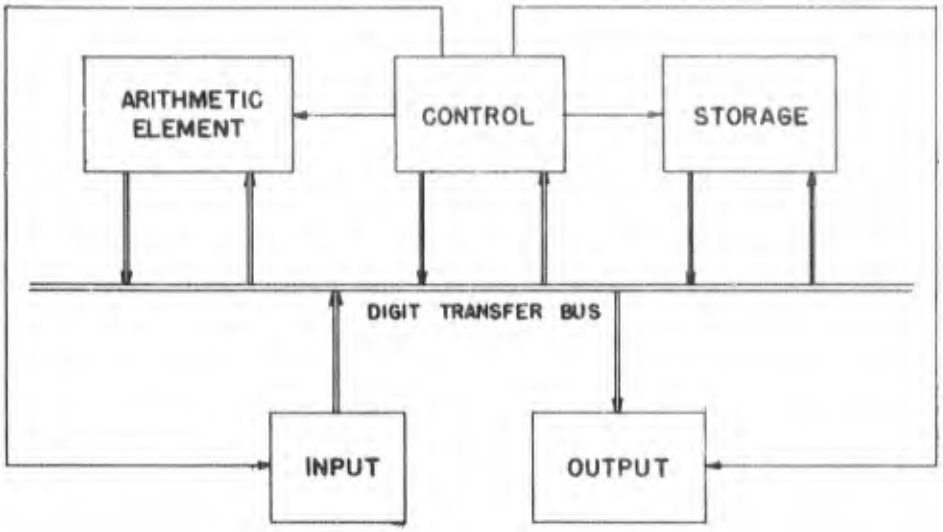

Figure 1

GENERAL BLOCK DIAGRAM

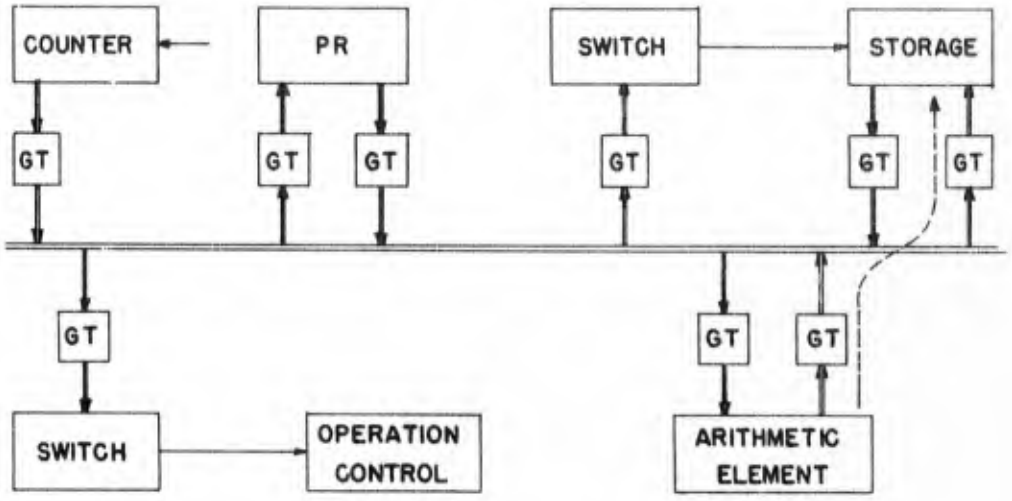

Figure 2

STORE RESULT

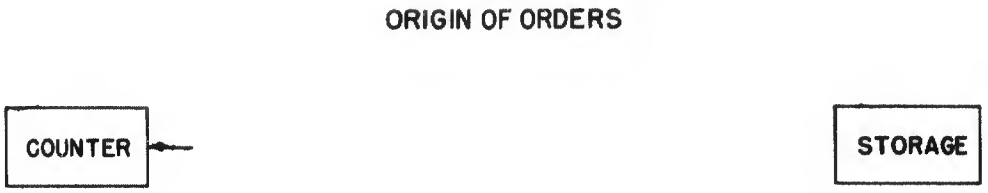

Figure 3
ORIGIN OF ORDERS

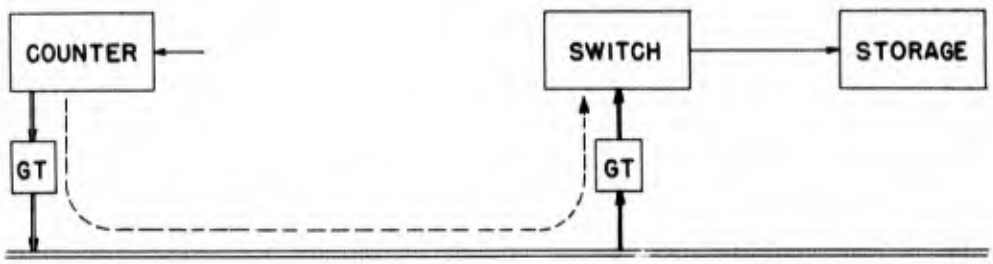

Figure 4
SETUP ORDER

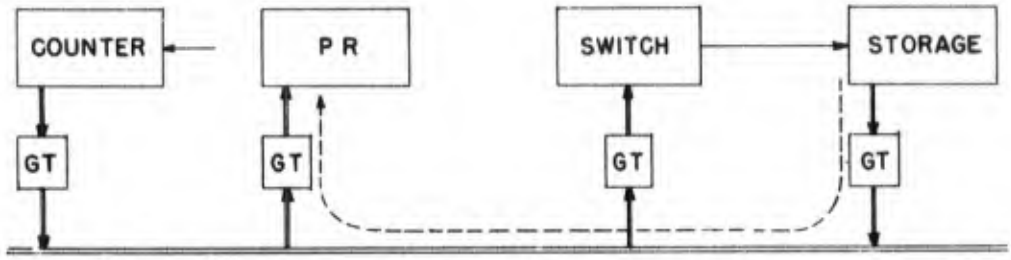

Figure 5
READ OUT ORDER

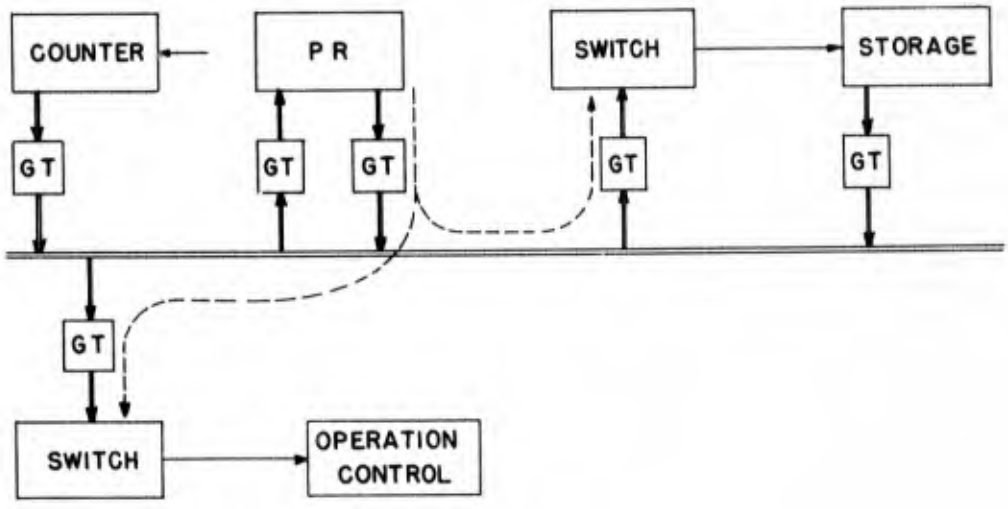

Figure 6
SETUP OPERATION

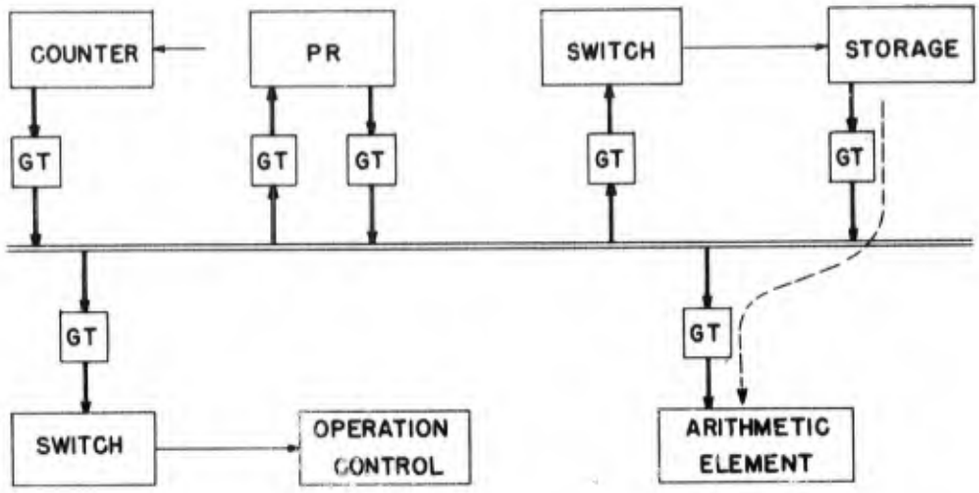

Figure 7

PERFORM OPERATION

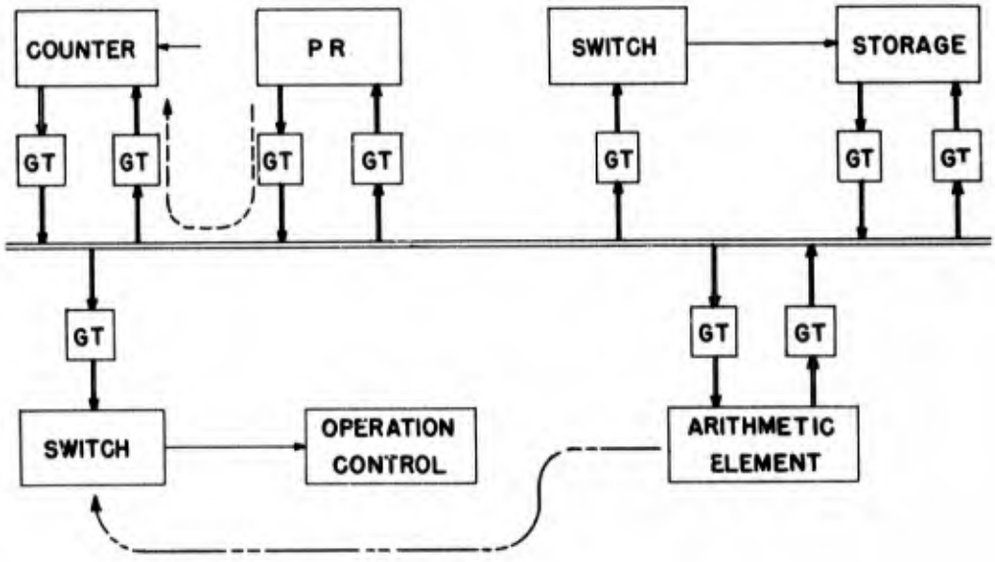

Figure 8

SUBPROGRAM

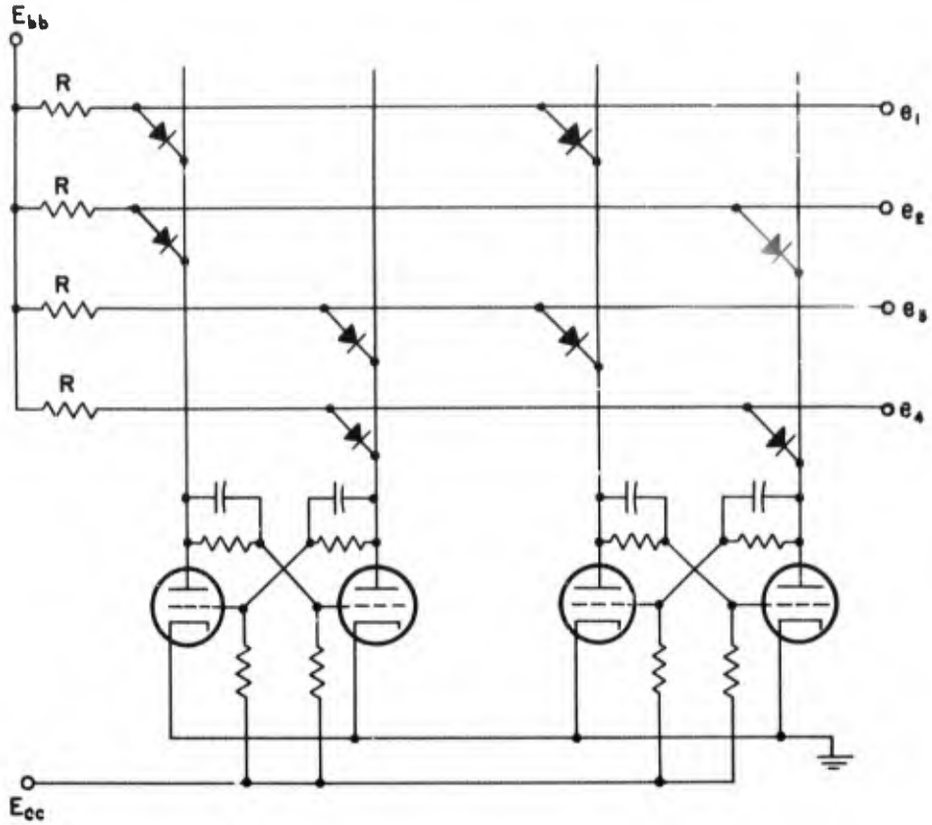

Figure 9

ELECTRONIC SWITCH

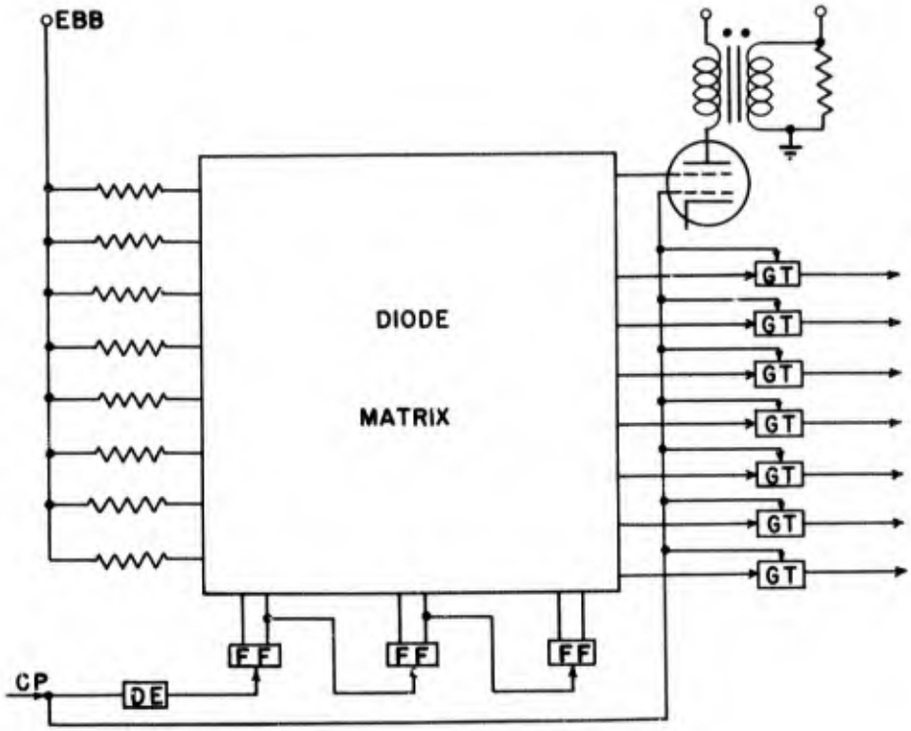

Figure 10

TIME PULSE DISTRIBUTOR

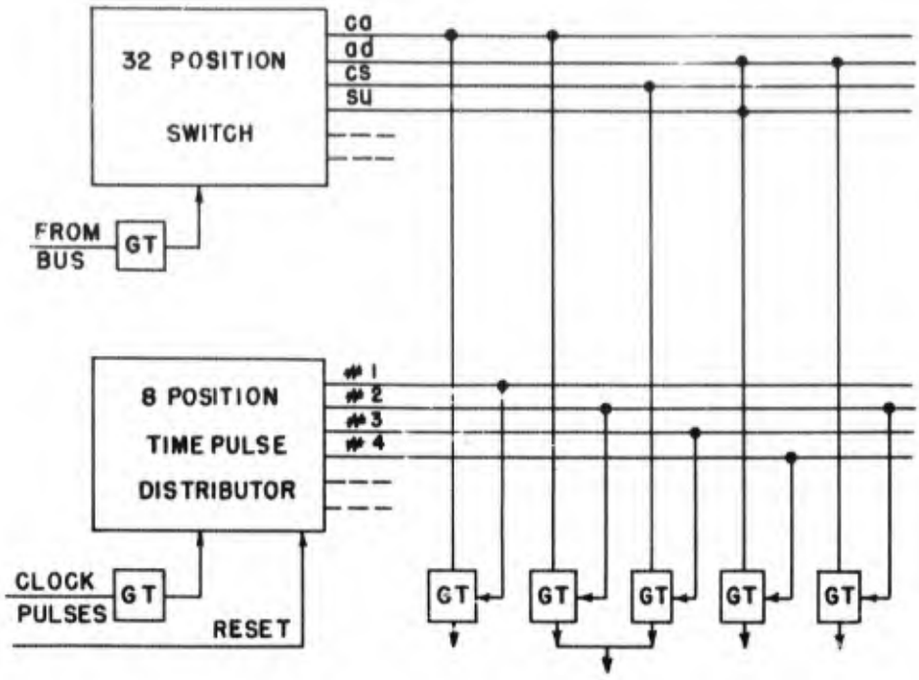

Figure 11

CONTROL

```
 3546
 1371
 ----
   1
 4817
   +1
 ----
 4917
```

Figure 12

DECIMAL ADDITION

```
 11011010
 10110110
 ---------
 01101100
  1  1  1
 ---------
 10100100
    1  1
 ---------
 10000000
    1  1
 ---------
 11001000
```

Figure 13
BINARY ADDITION

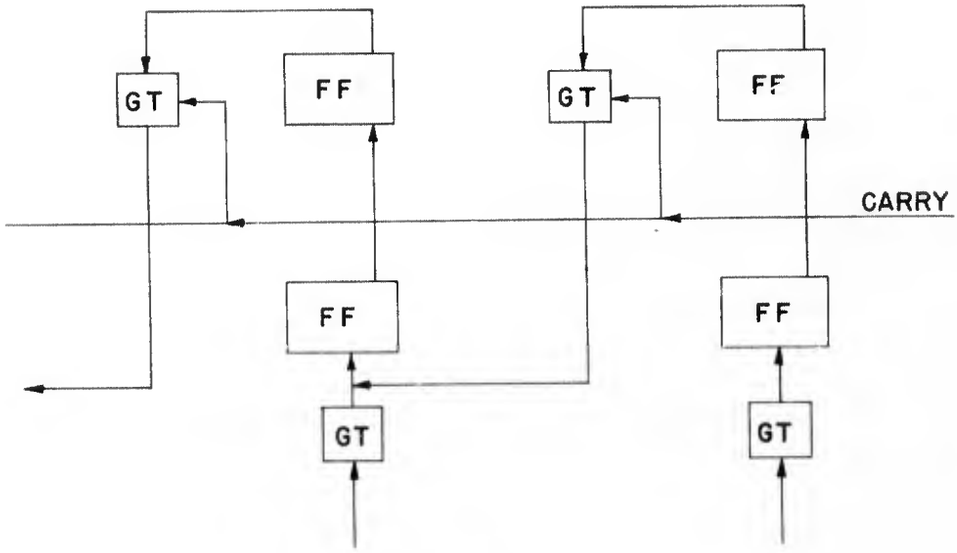

Figure 14
A BINARY ADDER

	DECIMAL	BINARY
POSITIVE NUMBER	223	11011111
NEGATIVE "	- 223	- 11011111
10's COMPLEMENT	1|777	1|00100001
9's "	1|776	1|00100000

Figure 15

NEGATIVE NUMBERS

BINARY			DECIMAL
+010110110	$= N_1$		- 182
-011010010	$= -N_2$		- -210
			- 28
010110110	$= N_1$		
100101101	$= 2^n - N_2 - 1$		
111100011	$= 2^n - (N_2 - N_1) - 1$		
-000011100	$= N_1 - N_2$		- -28
010110110	$= N_1$		- 182
-010010010	$= N_2$		- -146
			+ 36
010110110	$= N_1$		
101101101	$= 2^n - N_2 - 1$		
1000100011	$= N_1 - N_2 + 2^n - 1$		
END AROUND CARRY +1			
000100100	$= N_1 - N_2$		- + 36

Figure 16

SUBTRACTION USING 9'S COMPLEMENTS

```
  356   MULTIPLICAND
  627   MULTIPLIER
 -----
   42
   35
  21
 -----
 2492   PARTIAL PRODUCT
   12
  10
   6
 -----
 9612   PARTIAL PRODUCT
   36
  30
 18
-----
223212   PRODUCT
```

Figure 17

DECIMAL MULTIPLICATION

REPRESENTS POWERS OF 2

MULTIPLICATION TABLE:

1 X 1 = 1
1 X 0 = 0
0 X 0 = 0

ADDITION:

1 + 1 = 10
1 + 0 = 1
0 + 0 = 0

BINARY COLUMNS $\approx 3\frac{1}{3}$ X DECIMAL COLUMNS

ONLY DIGITS 1 AND 0 REQUIRED IN EQUIPMENT

Figure 18

BINARY NOTATION

```
  10110   MULTIPLICAND      22
  10011   MULTIPLIER        19
 -----                     ----
  10110                     198
 10110                      22
-------                   ----
 1000010  PARTIAL PRODUCT   418
00000
-------
 1000010  PARTIAL PRODUCT
00000
-------
 01000010 PARTIAL PRODUCT
10110
-------
110100010  = 418 PRODUCT
```

Figure- 19

BINARY MULTIPLICATION

```
          10110   MULTIPLICAND
STEP 1    10011   MULTIPLIER
          10110   PARTIAL PRODUCT
          ---------------------
          10110   MULTIPLICAND
           1001   SHIFTED MULTIPLIER
STEP 2    10110   SHIFTED PARTIAL PRODUCT
          10110
          -------
          1000010 PARTIAL PRODUCT
          ---------------------
          10110   MULTIPLICAND
            100   SHIFTED MULTIPLIER
STEP 3    1000010 SHIFTED PARTIAL PRODUCT
          00000
          -------
          1000010 PARTIAL PRODUCT
          ---------------------
          10110   MULTIPLICAND
             10   SHIFTED MULTIPLIER
STEP 4    1000010 SHIFTED PARTIAL PRODUCT
          00000
          -------
          01000010 PARTIAL PRODUCT
          ---------------------
          10110   MULTIPLICAND
              1   SHIFTED MULTIPLIER
STEP 5    01000010 SHIFTED PARTIAL
          10110          PRODUCT
          -------
          110100010 PRODUCT
```

Figure 20

MODIFIED BINARY MULTIPLICATION

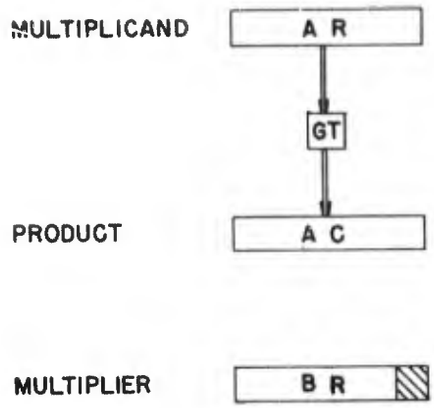

Figure 21

MULTIPLICATION I

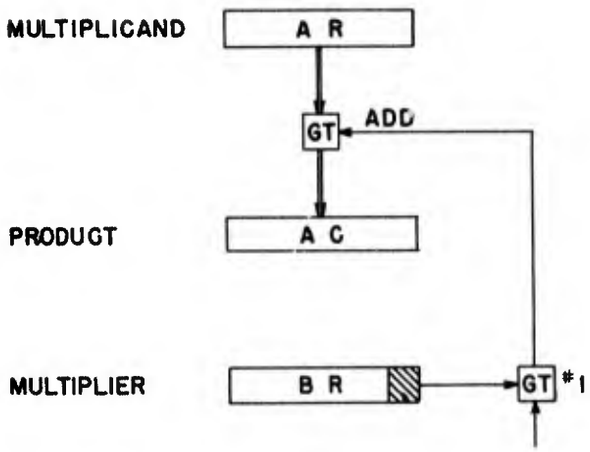

Figure 22

MULTIPLICATION II

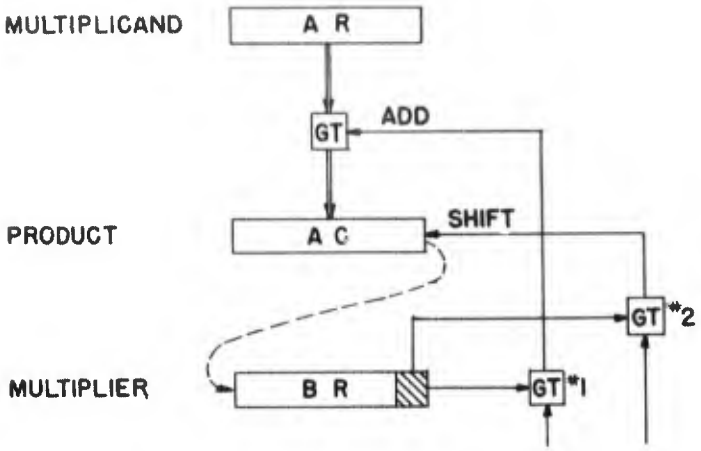

Figure 23
MULTIPLICATION III

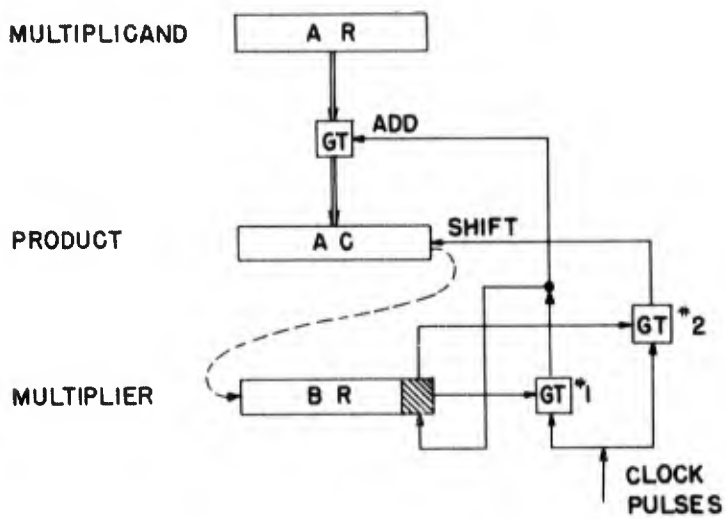

Figure 24
MULTIPLICATION IV

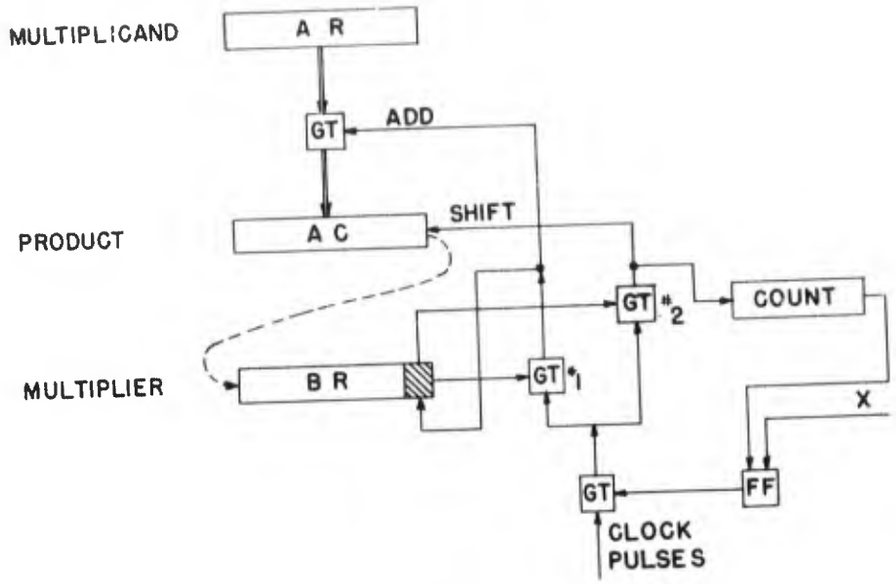

Figure 25
MULTIPLICATION V

DECIMAL

1734	6148
	5
1735	1

173	46148
	5
173	9

BINARY

11010	1010
	1
11011	

1101	01010
	1
1101	1

Figure 26
ROUNDING OFF

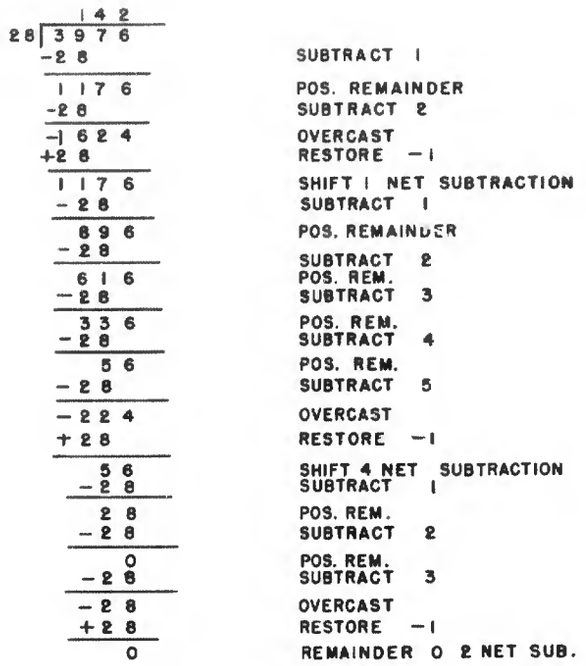

Figure 27

DECIMAL DIVISION

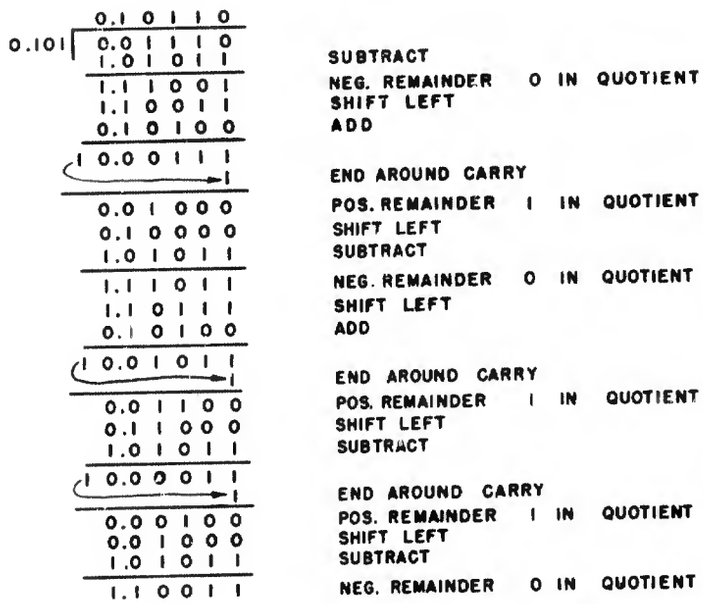

Figure 28

BINARY DIVISION

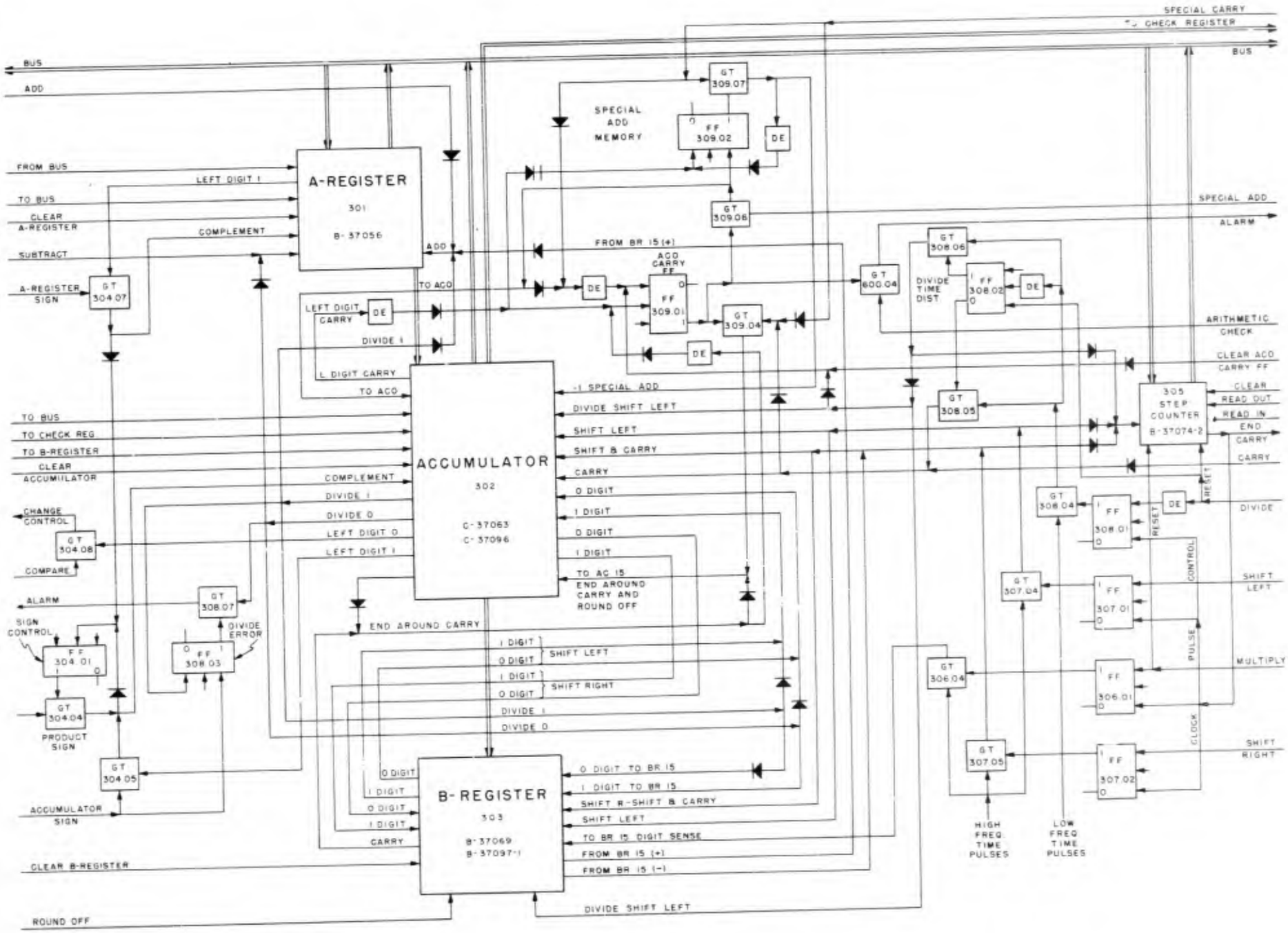

Figure 29

ARITHMETIC ELEMENT

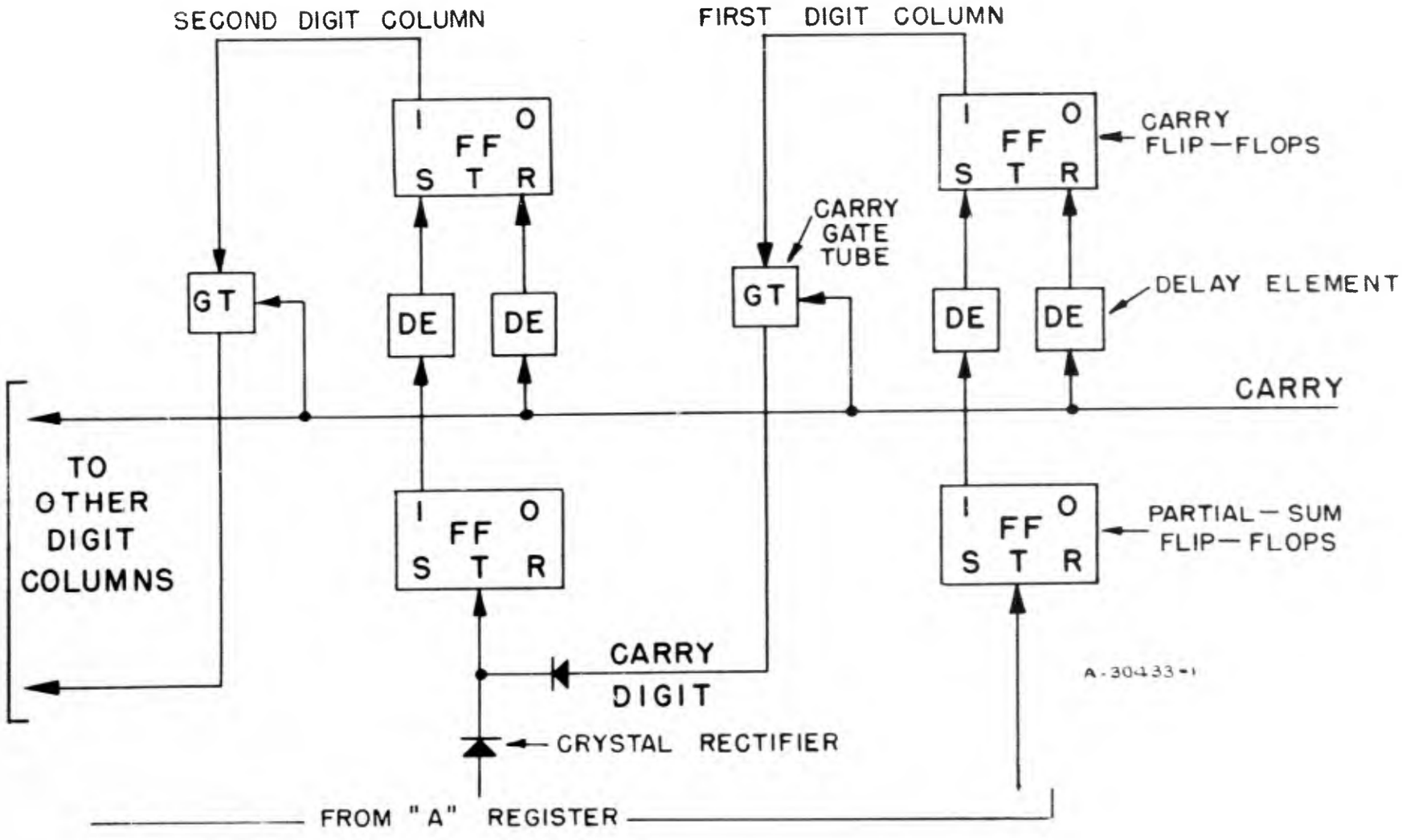

Figure 30

ACCUMULATOR

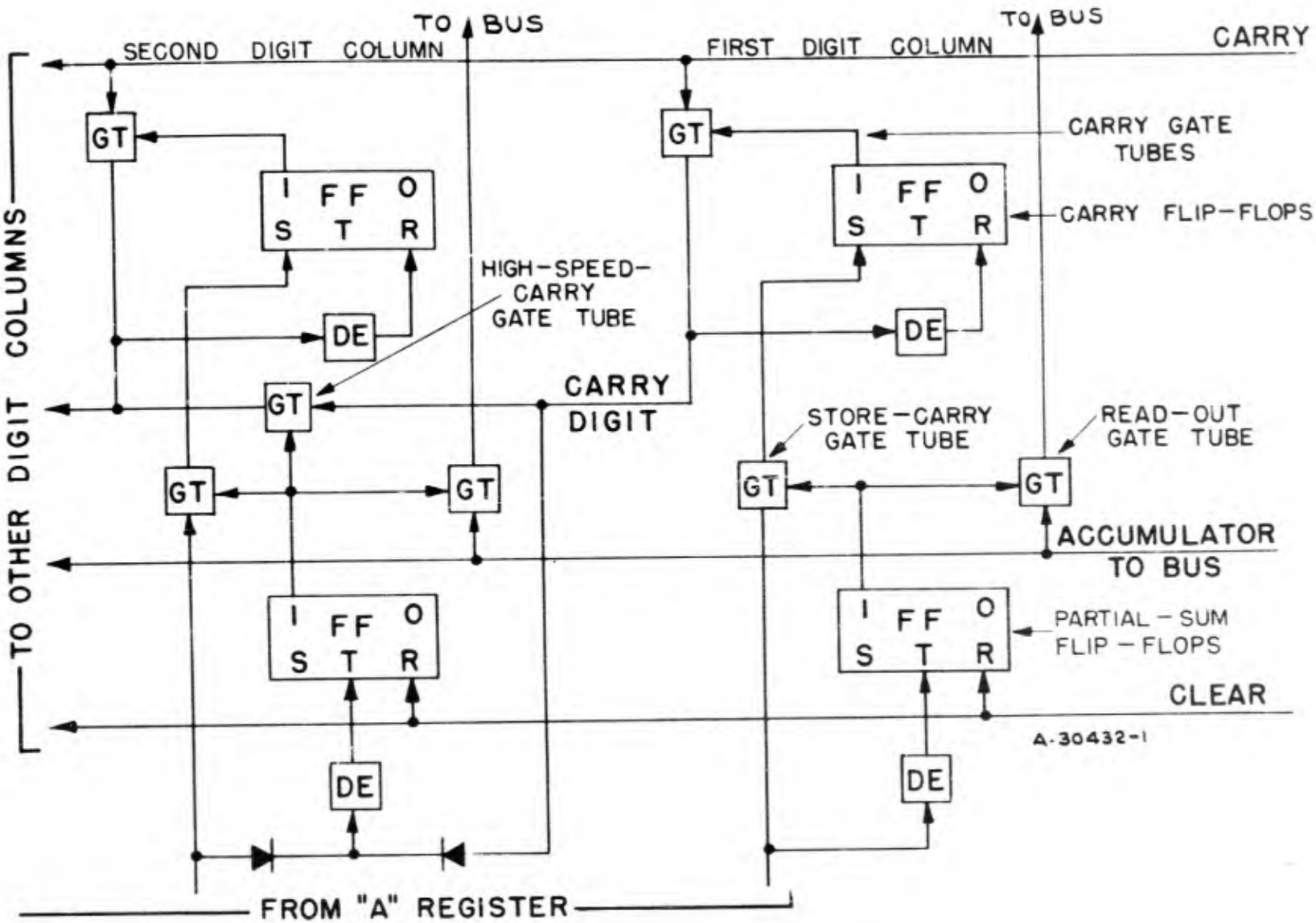

Figure 31
ACCUMULATOR

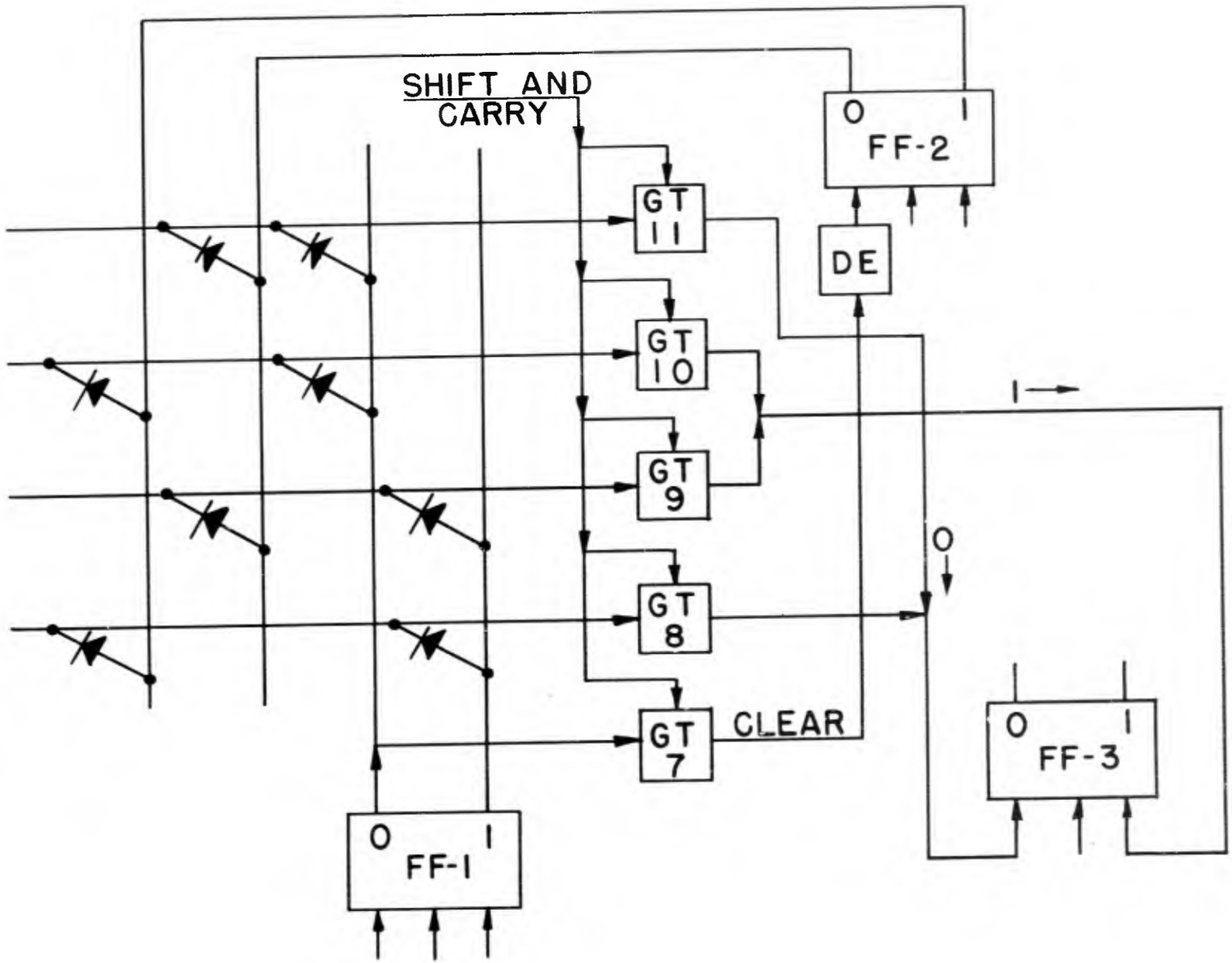

Figure 32
SHIFT AND CARRY

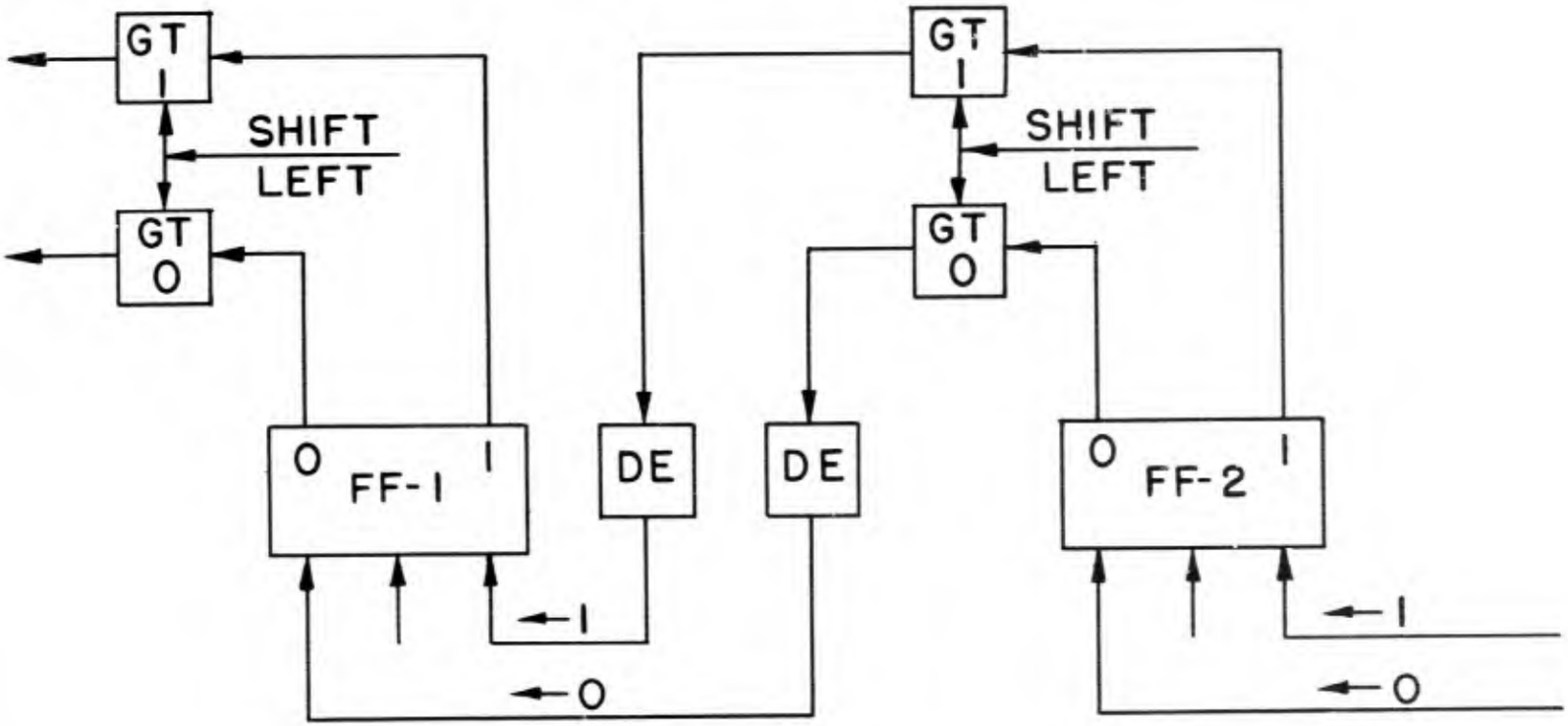

Figure 33
SHIFT LEFT

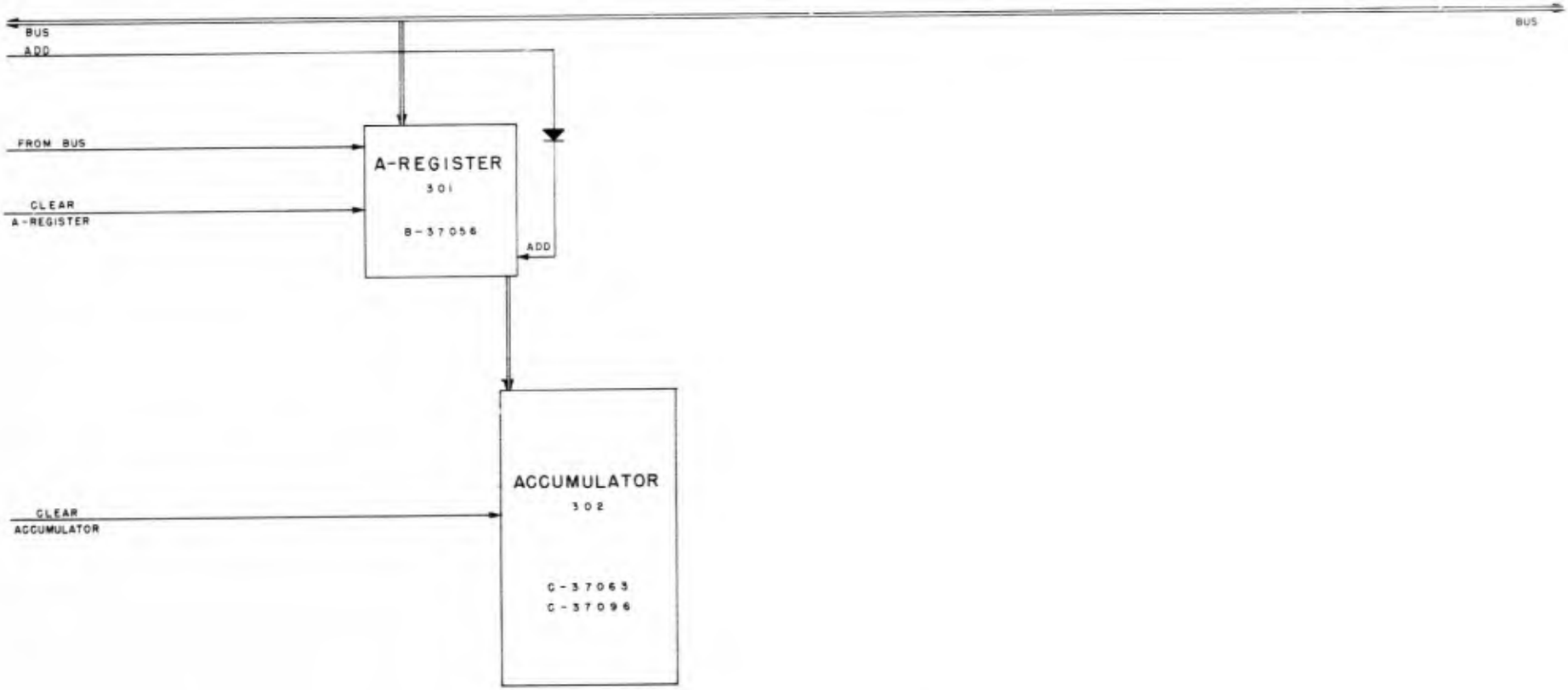

Figure 34
CLEAR AND ADD

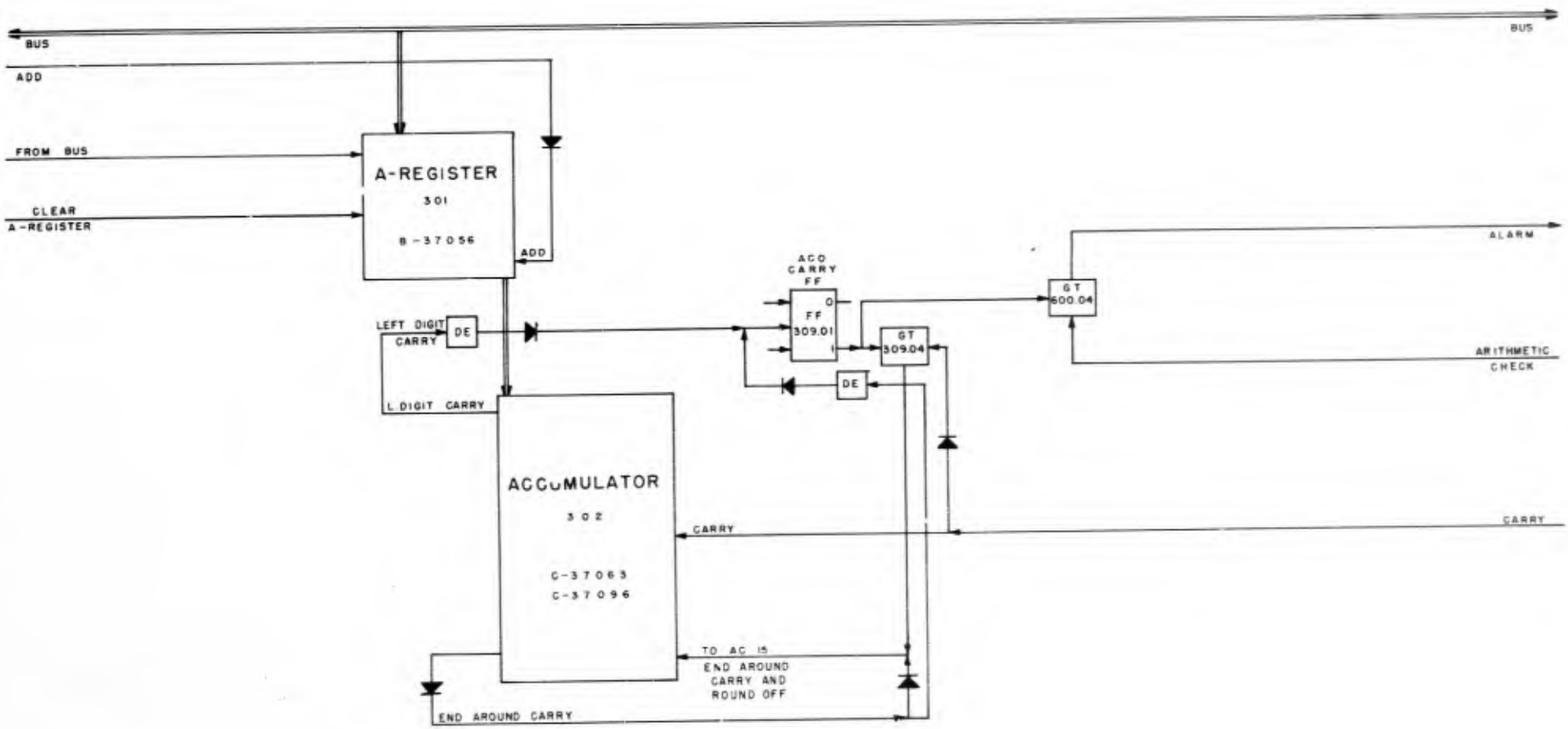

Figure 35
ADD

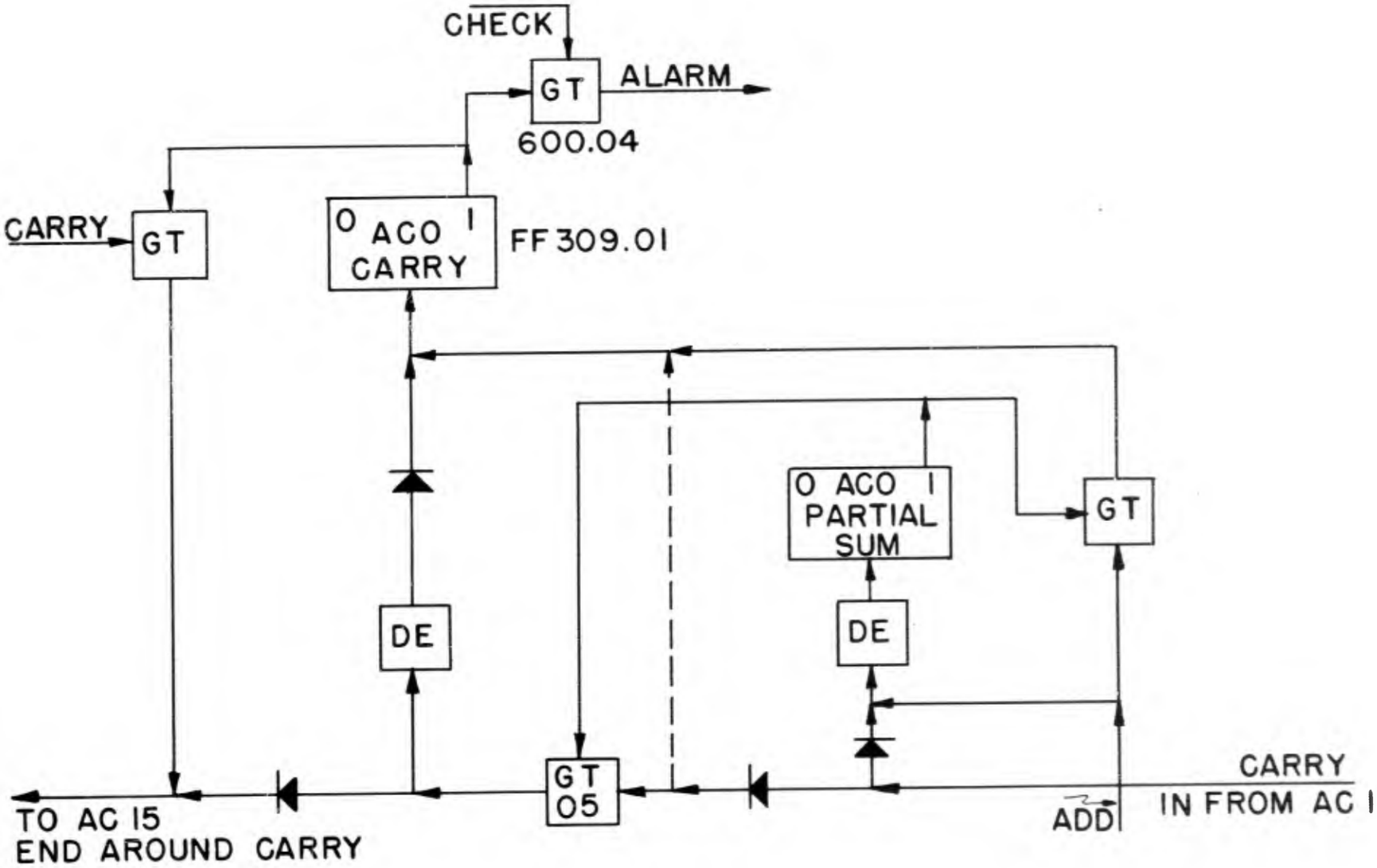

Figure 36
ARITHMETIC CHECK

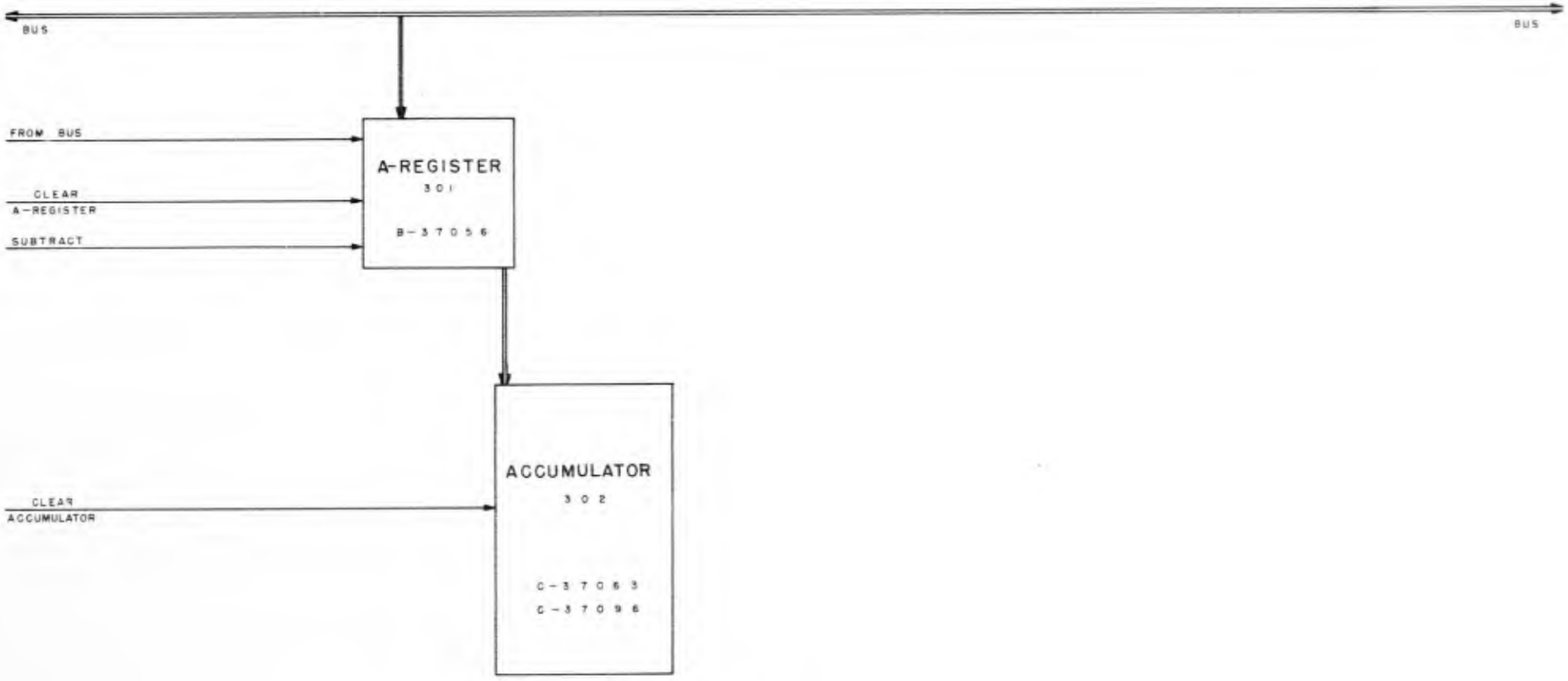

Figure 37

CLEAR AND SUBTRACT

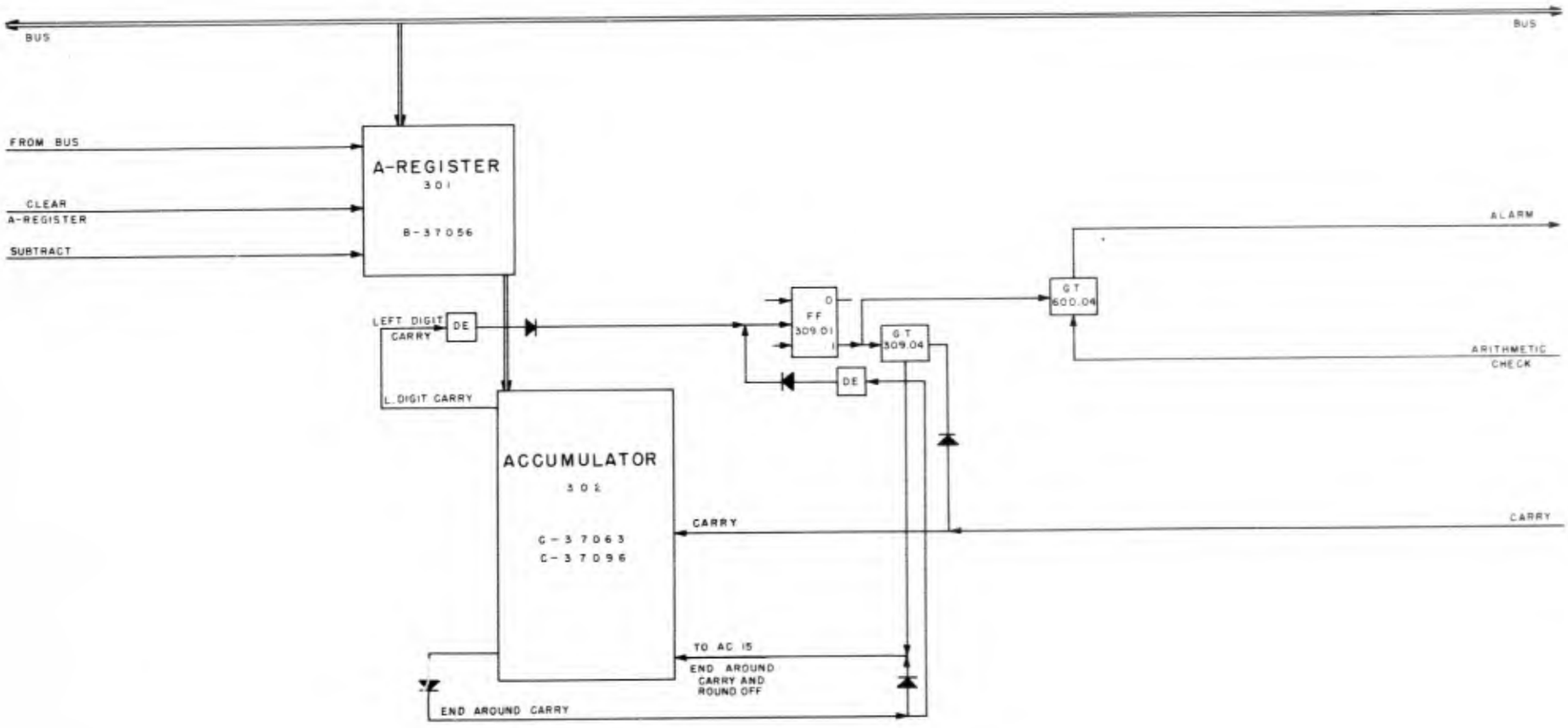

Figure 38
SUBTRACT

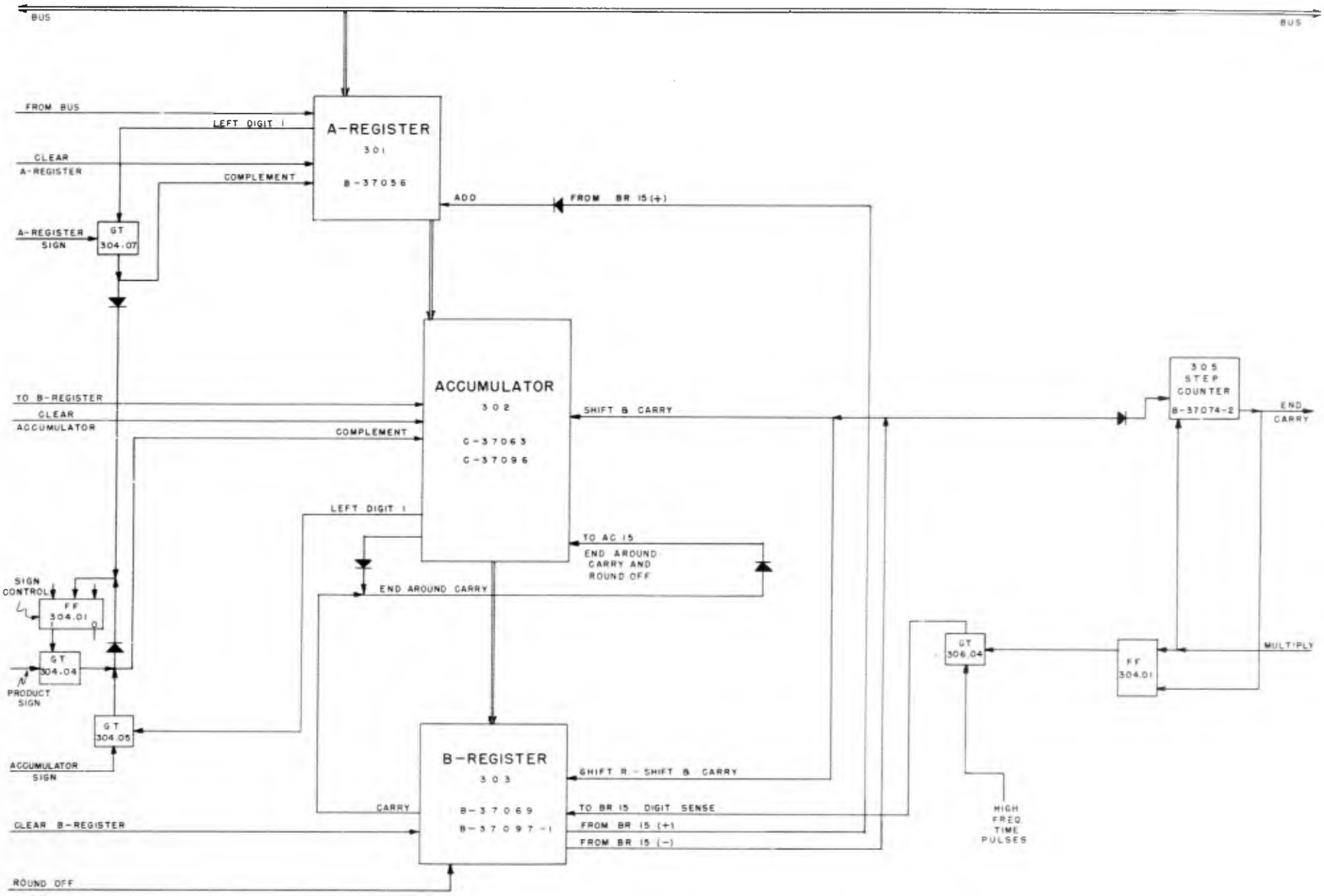

Figure 39

MULTIPLY AND ROUNDOFF

MULTIPLY AND HOLD FULL PRODUCT

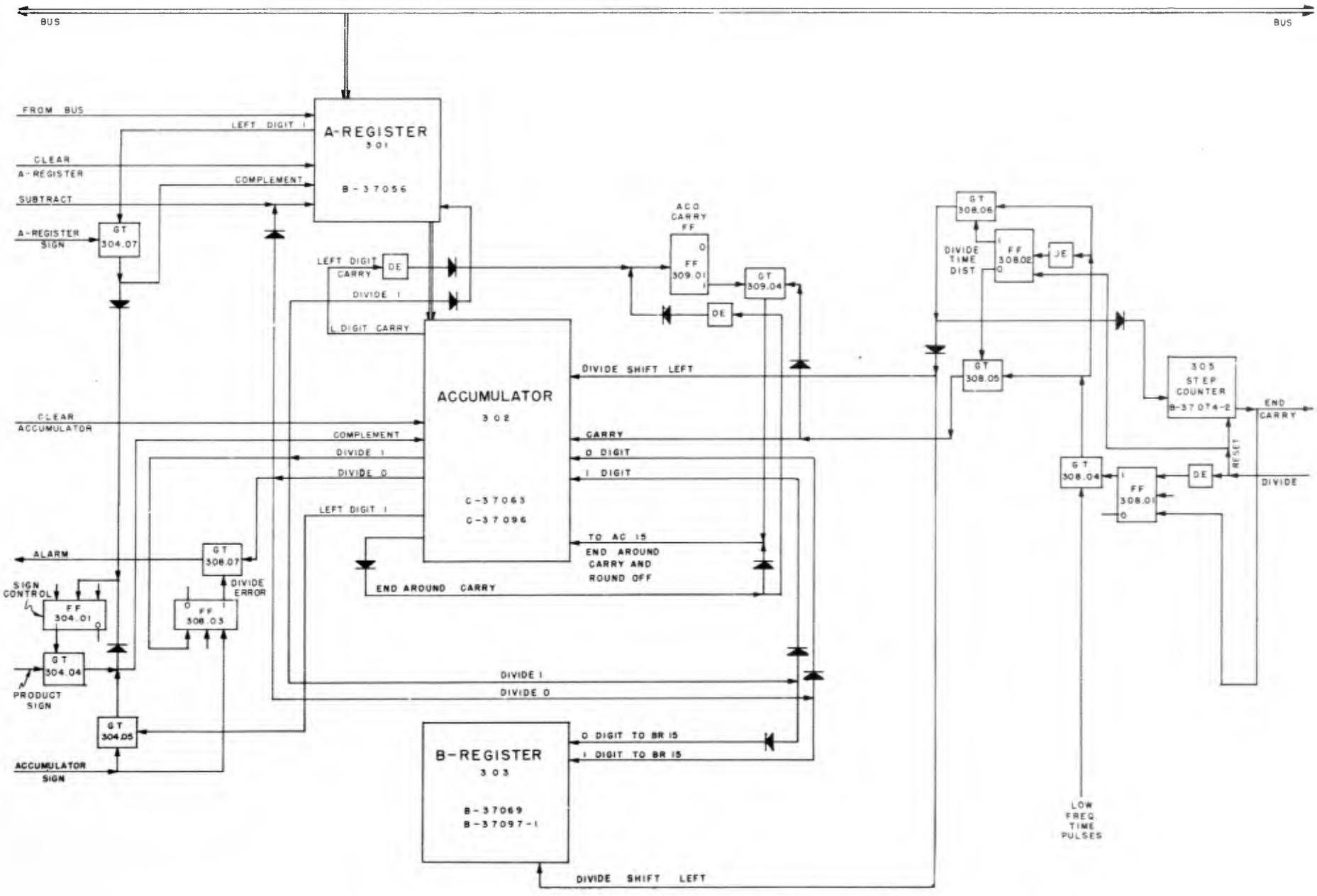

Figure 40

DIVIDE

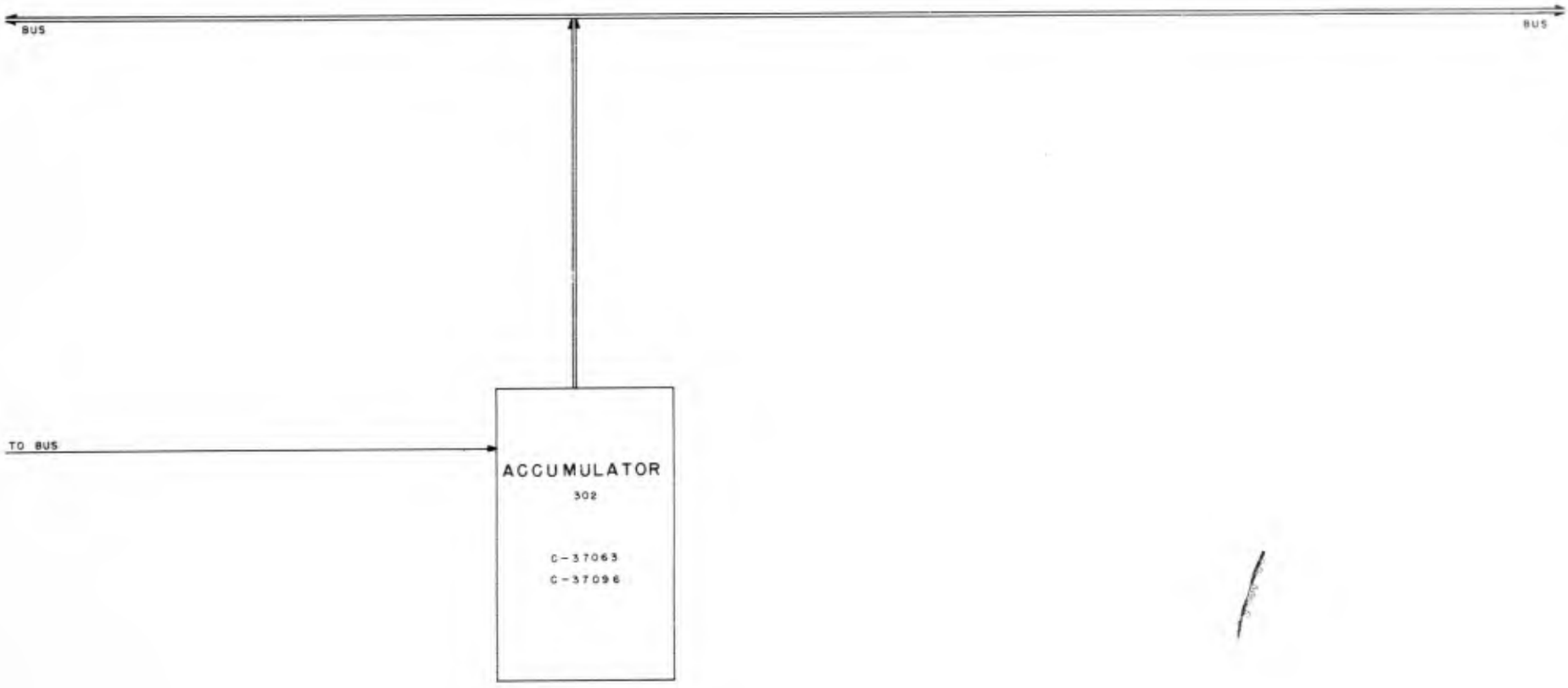

Figure 41

TRANSFER TO STORAGE

TRANSFER DIGITS

STORE AND DISPLAY

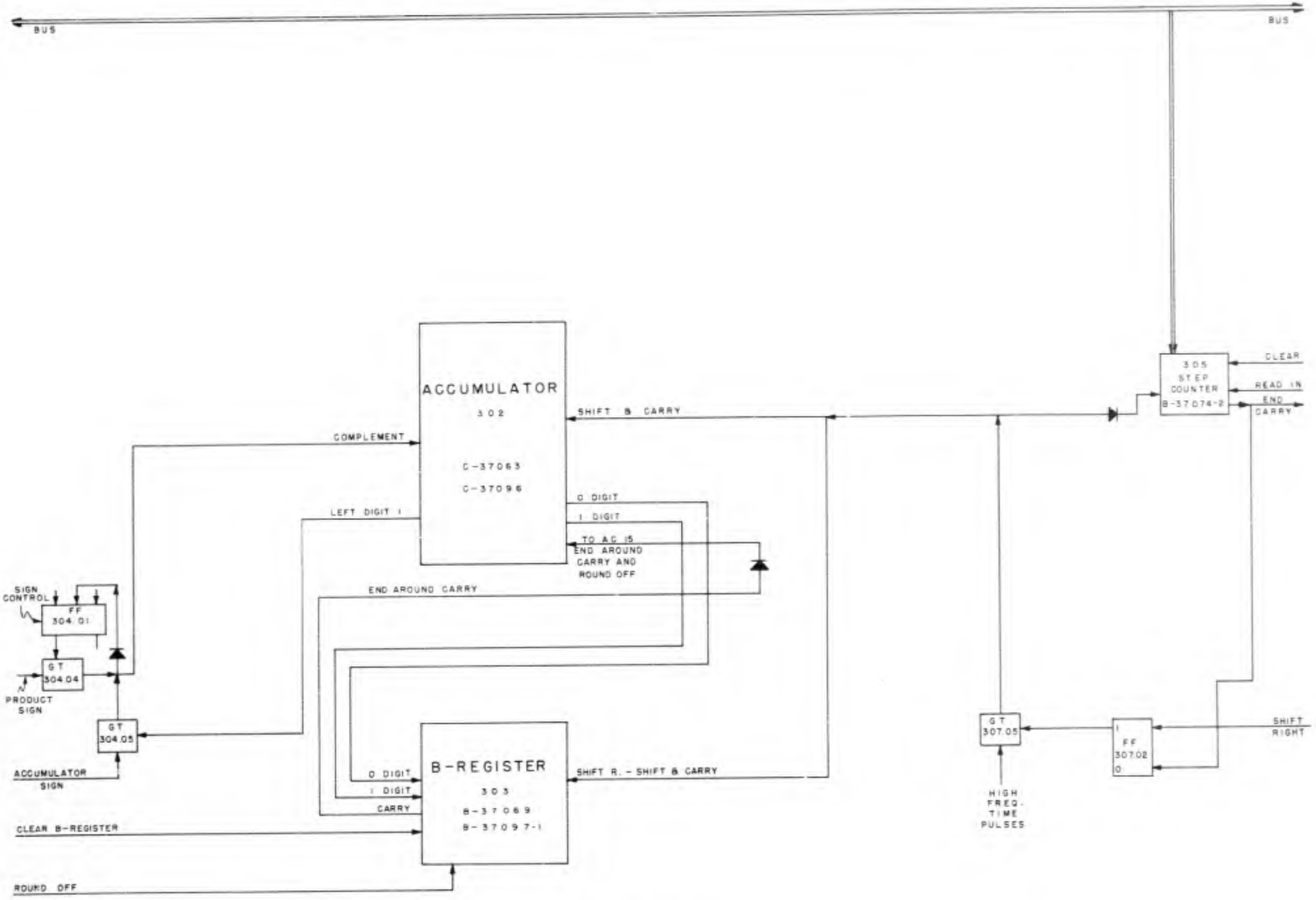

Figure 42

SHIFT RIGHT

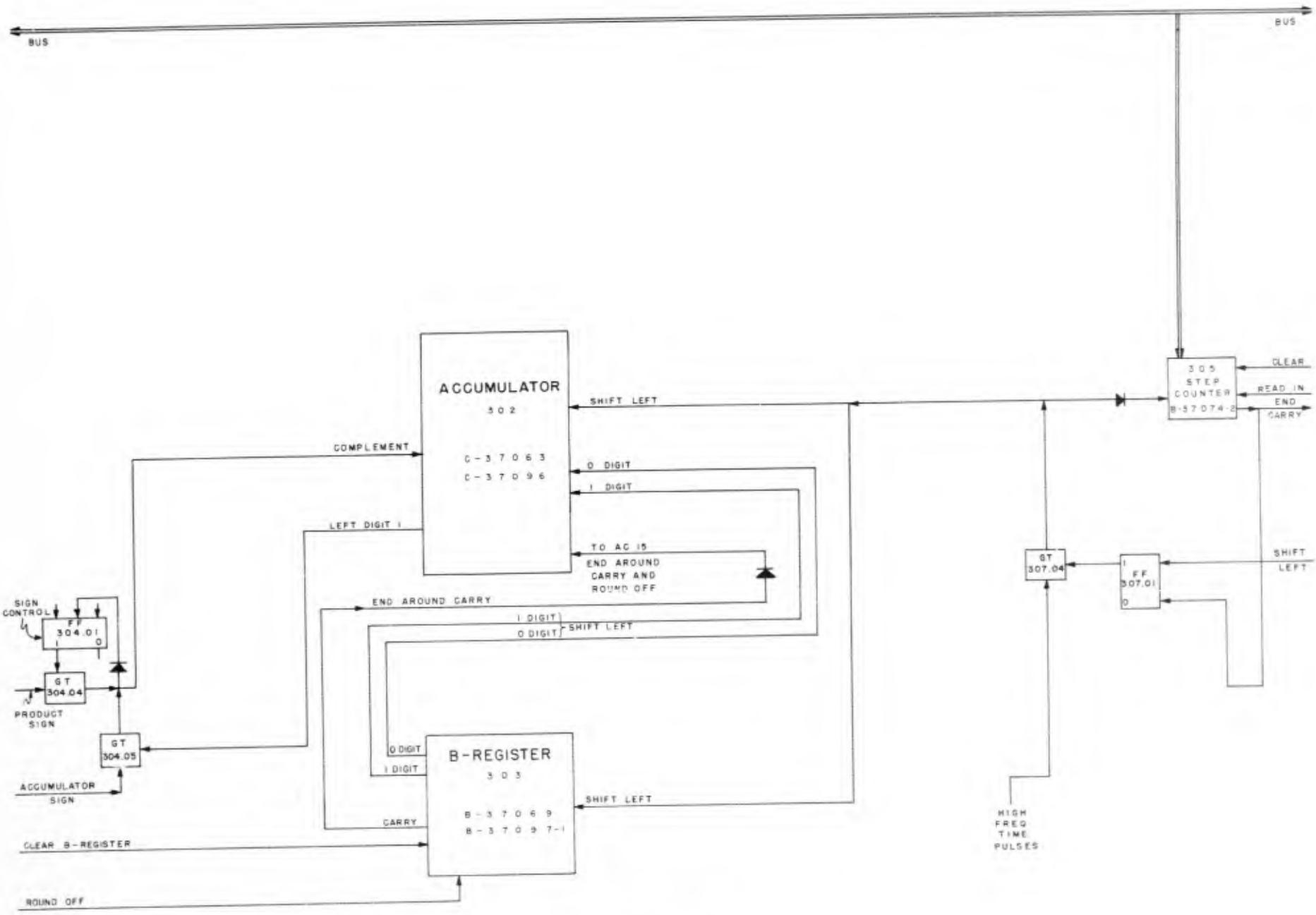

Figure 43

SHIFT LEFT

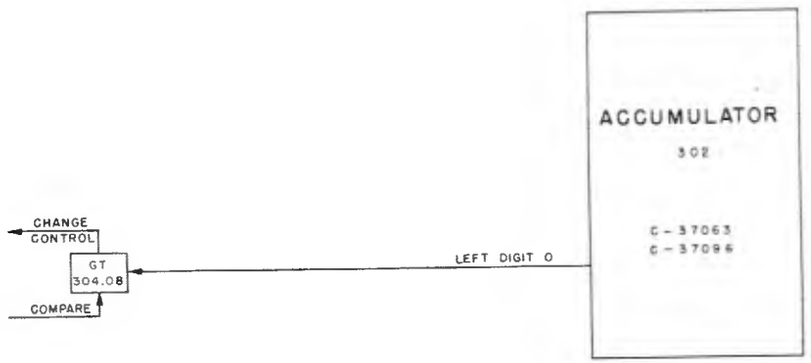

Figure 44
CONDITIONAL PROGRAM

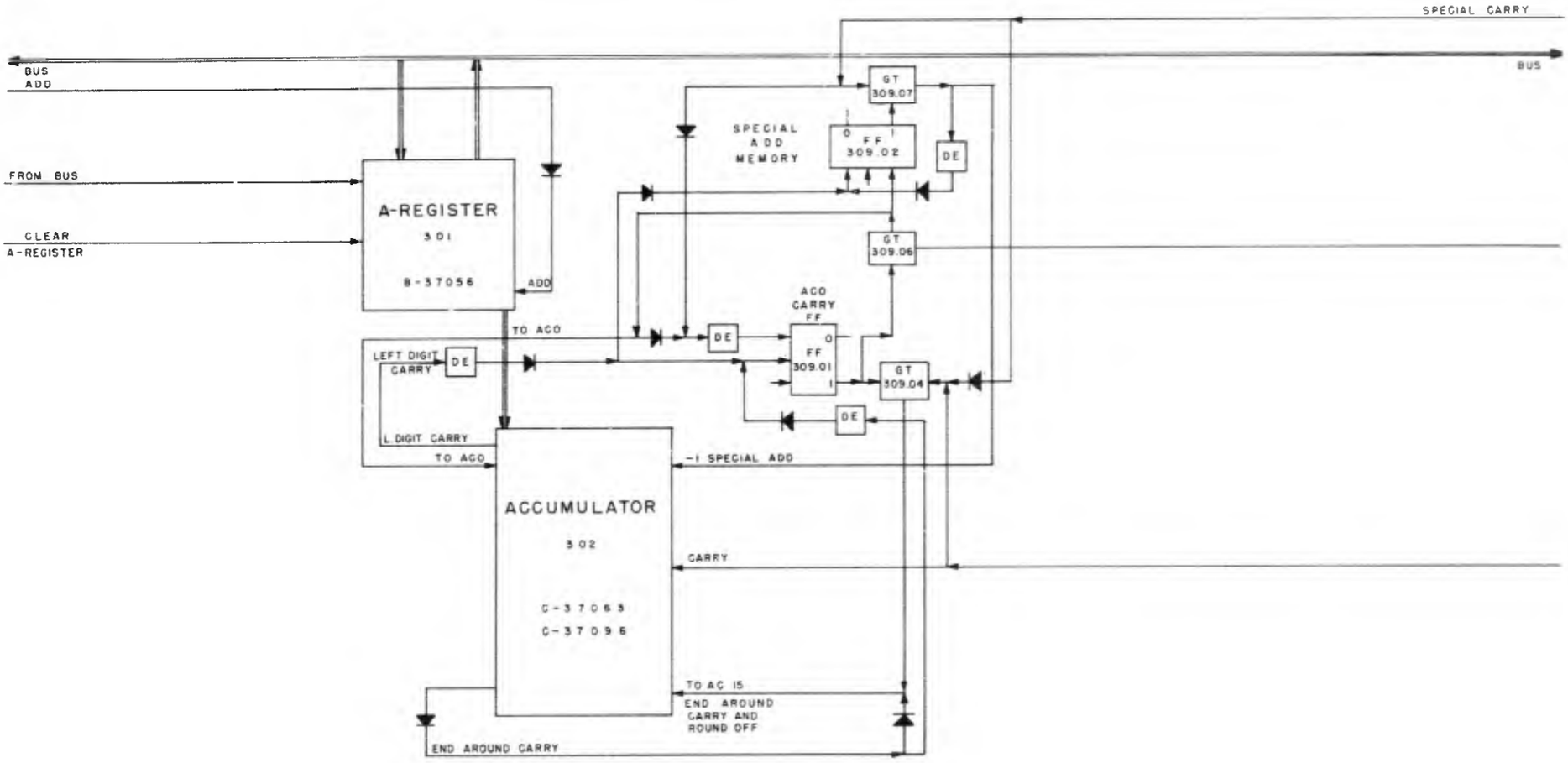

Figure 45
SPECIAL ADD

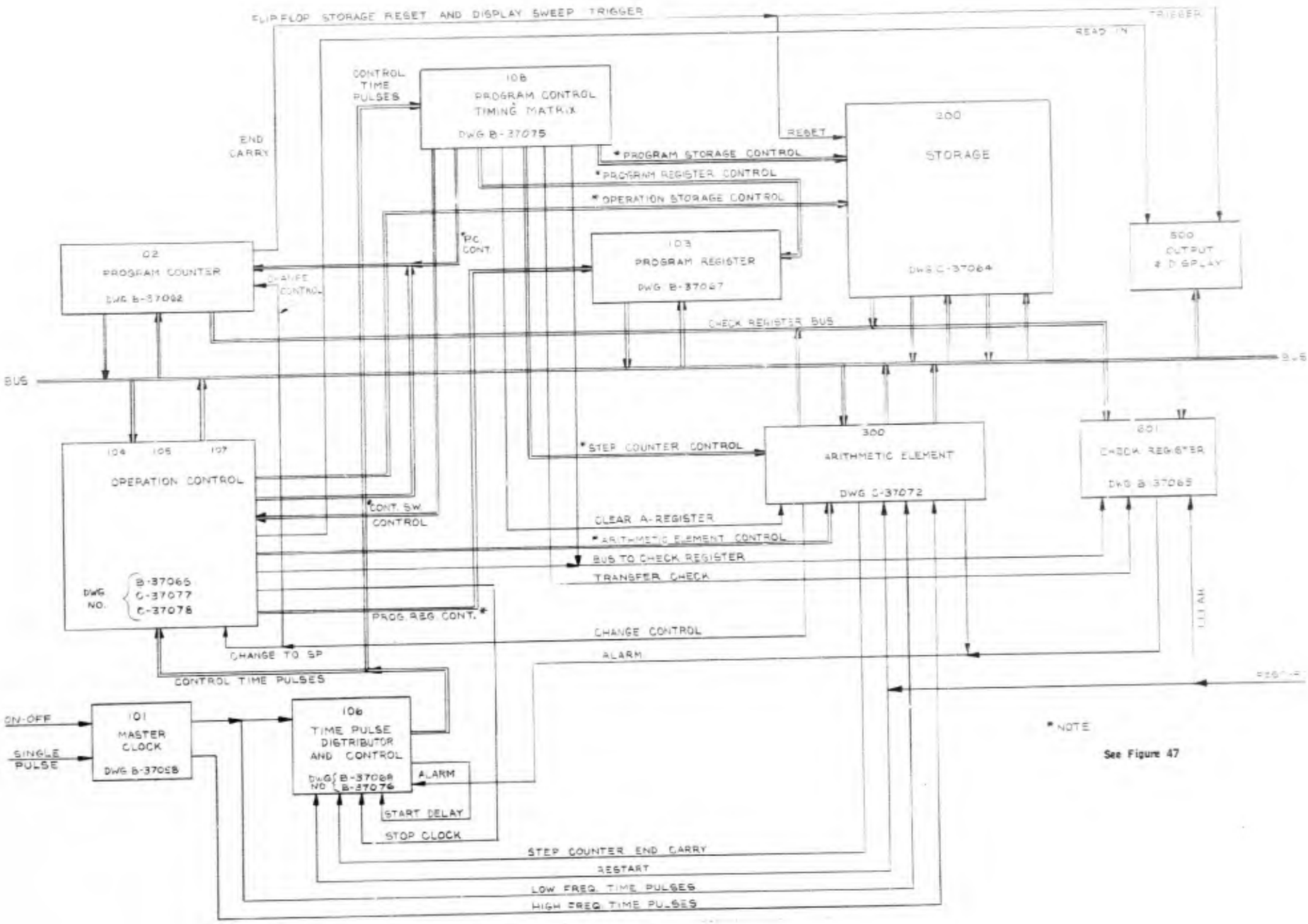

Figure 46

SYSTEM BLOCK DIAGRAM

ARITHMETIC ELEMENT CONTROL

1.	Bus to A-Register	GT 301.01
2.	A-Register to Bus	GT 301.02
3.	Subtract: A-Register to Accum.	GT 301.04
4.	Add: A-Register to Accumulator	GT 301.05
5.	Accumulator to Bus	GT 302.02
6.	Accumulator to Check Register	GT 302.03
7.	Accumulator to B-Register	GT 302.04
8.	Carry	GT 302.20
9.	Roundoff	GT 303.08
10.	Product Sign	GT 304.04
11.	Accumulator Sign	GT 304.05
12.	A-Register Sign	GT 304.07
13.	Compare	GT 304.08
14.	Multiply	FF 306.01
15.	Shift Left	FF 307.01
16.	Shift Right	FF 307.02
17.	Divide	FF 308.01
18.	Special Add	GT 309.06
19.	Arithmetic Check	GT 600.04
20.	Clear Accumulator	
21.	Clear B-Register	
22.	Special Carry	

PROGRAM COUNTER CONTROL

1.	In from Bus	GT 102.01
2.	Out to Bus	GT 102.02
3.	Out to Check Register	GT 102.03
4.	Add Pulse	
5.	Clear	

PROGRAM REGISTER CONTROL

1.	In from Bus	GT 103.01
2.	Out to Bus	GT 103.02
3.	Clear	

CONTROL SWITCH CONTROL

1.	In from Bus	GT 104.01
2.	Out to Bus	GT 104.02
3.	Clear	

STEP COUNTER CONTROL

1.	In from Bus	GT 305.01
2.	Out to Bus	GT 305.02
3.	Clear	

PROGRAM STORAGE CONTROL

1.	Bus to Storage Switch	GT 201.01
2.	Storage Switch to Bus	GT 201.02
3.	Storage Readout	GT 203.02
4.	Storage Switch Clear	
5.	Storage to Check Register	GT 203.03

OPERATION STORAGE CONTROL

1.	In from Bus	GT 203.01
2.	Storage Readout	GT 203.02
3.	Out to Check Register	GT 203.03
4.	Storage Clear	

NOTE: See Figure 46

Figure 47

CONTROL FUNCTIONS

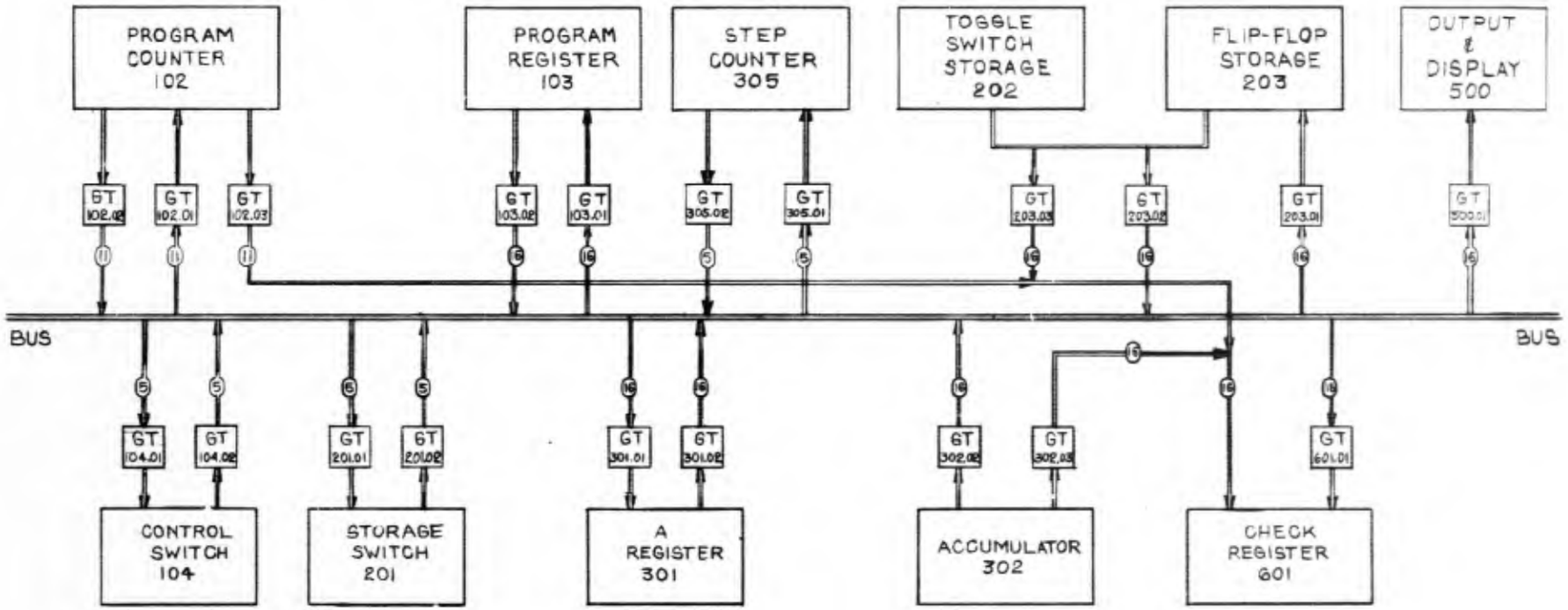

Figure 48

BUS CONNECTIONS

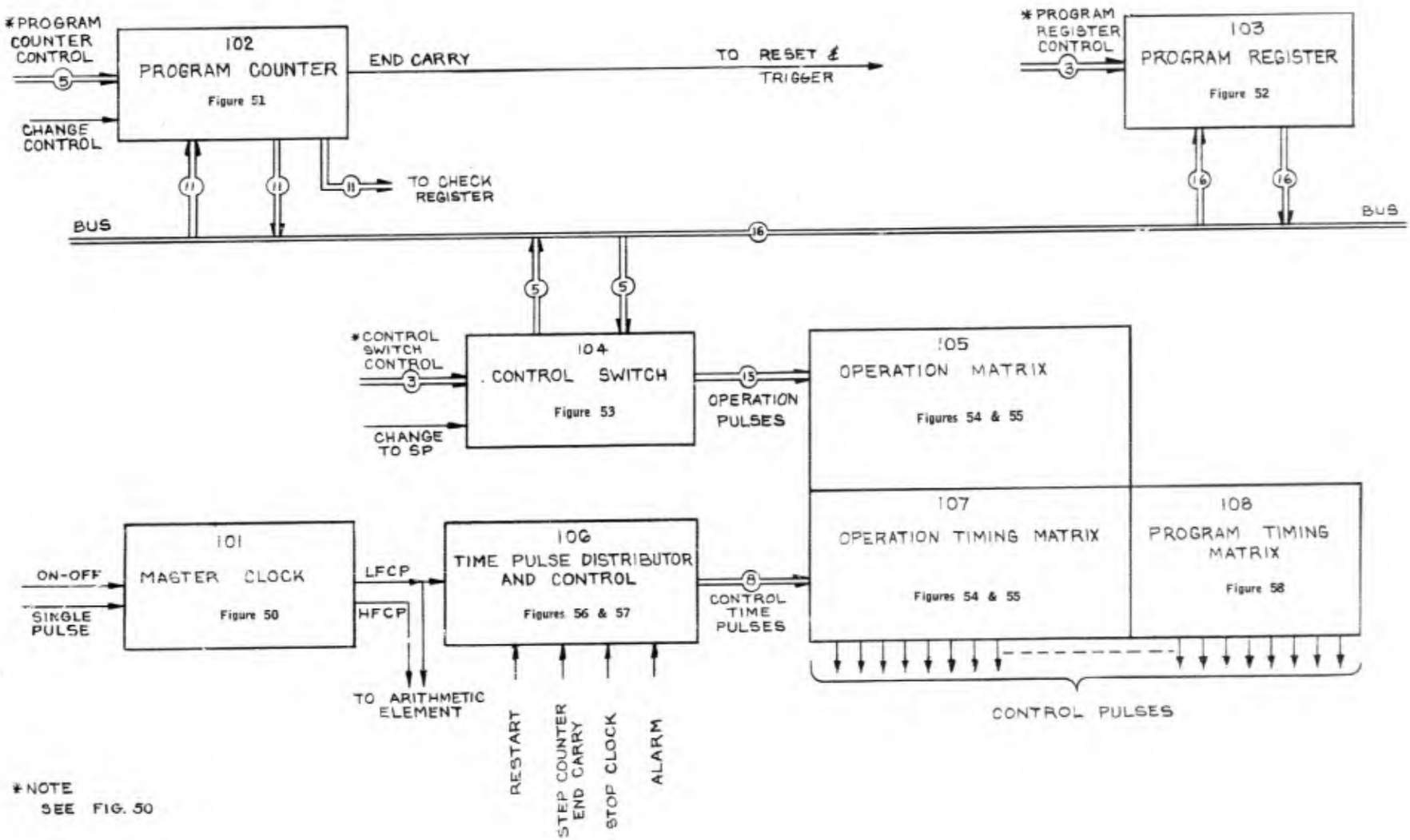

Figure 49

CONTROL

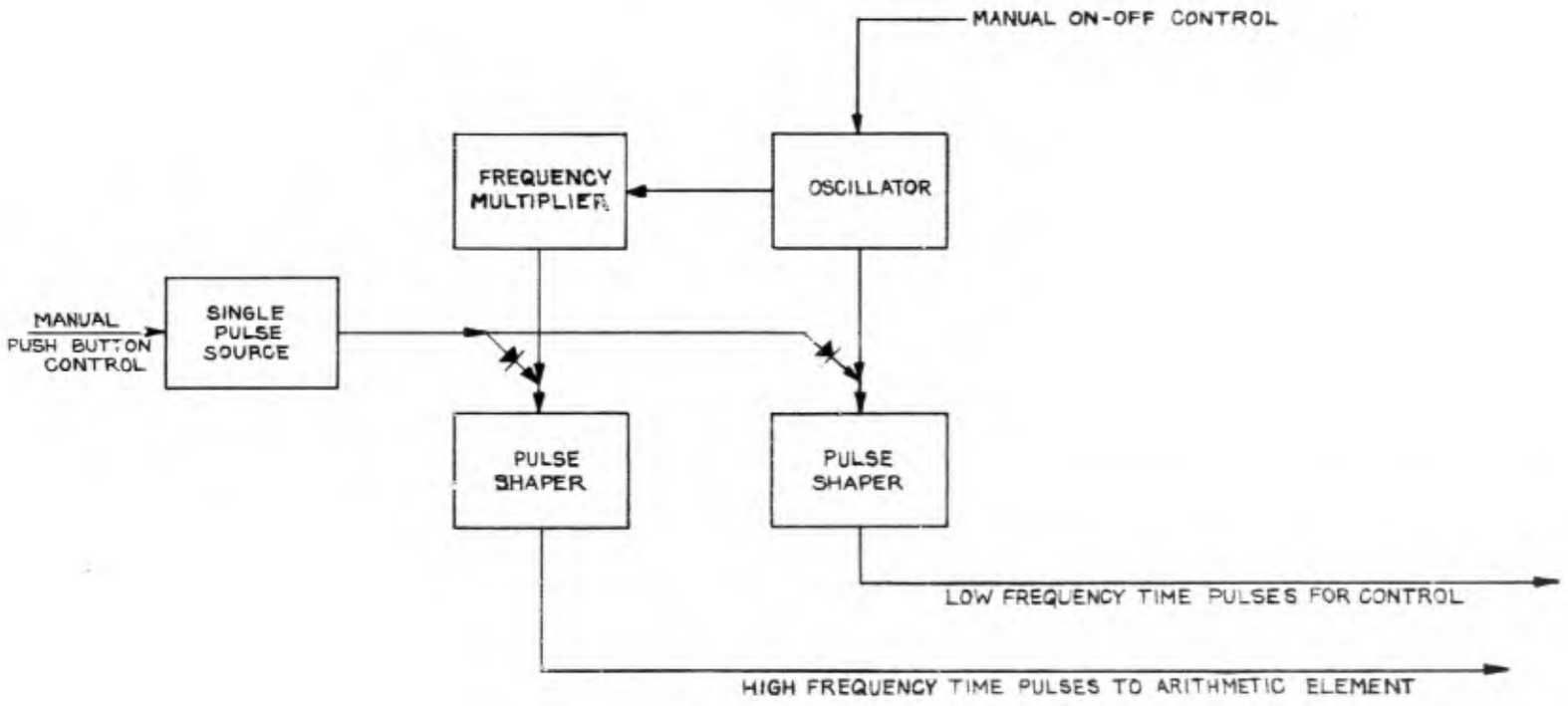

Figure 50
MASTER CLOCK

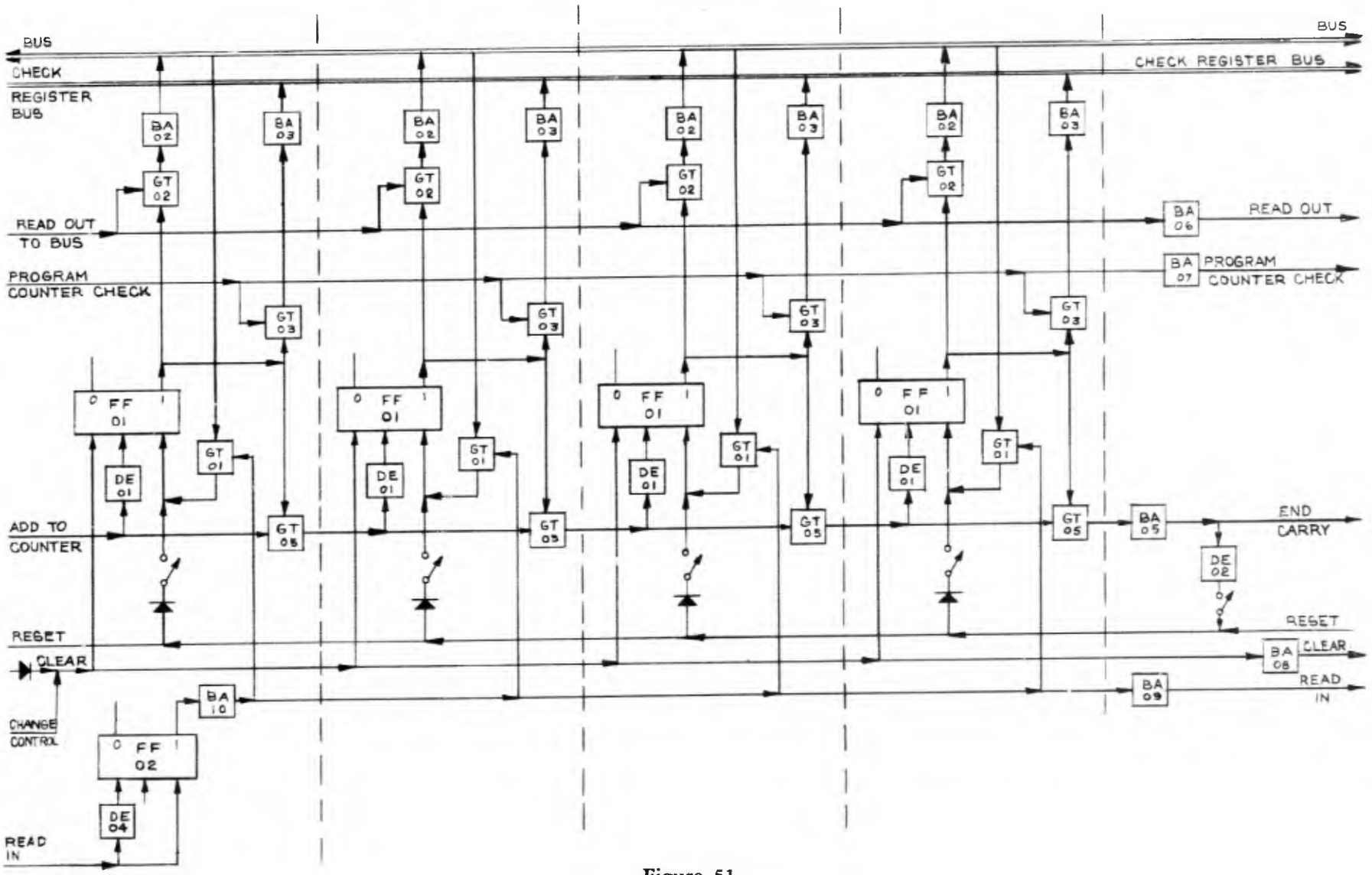

Figure 51

PROGRAM COUNTER

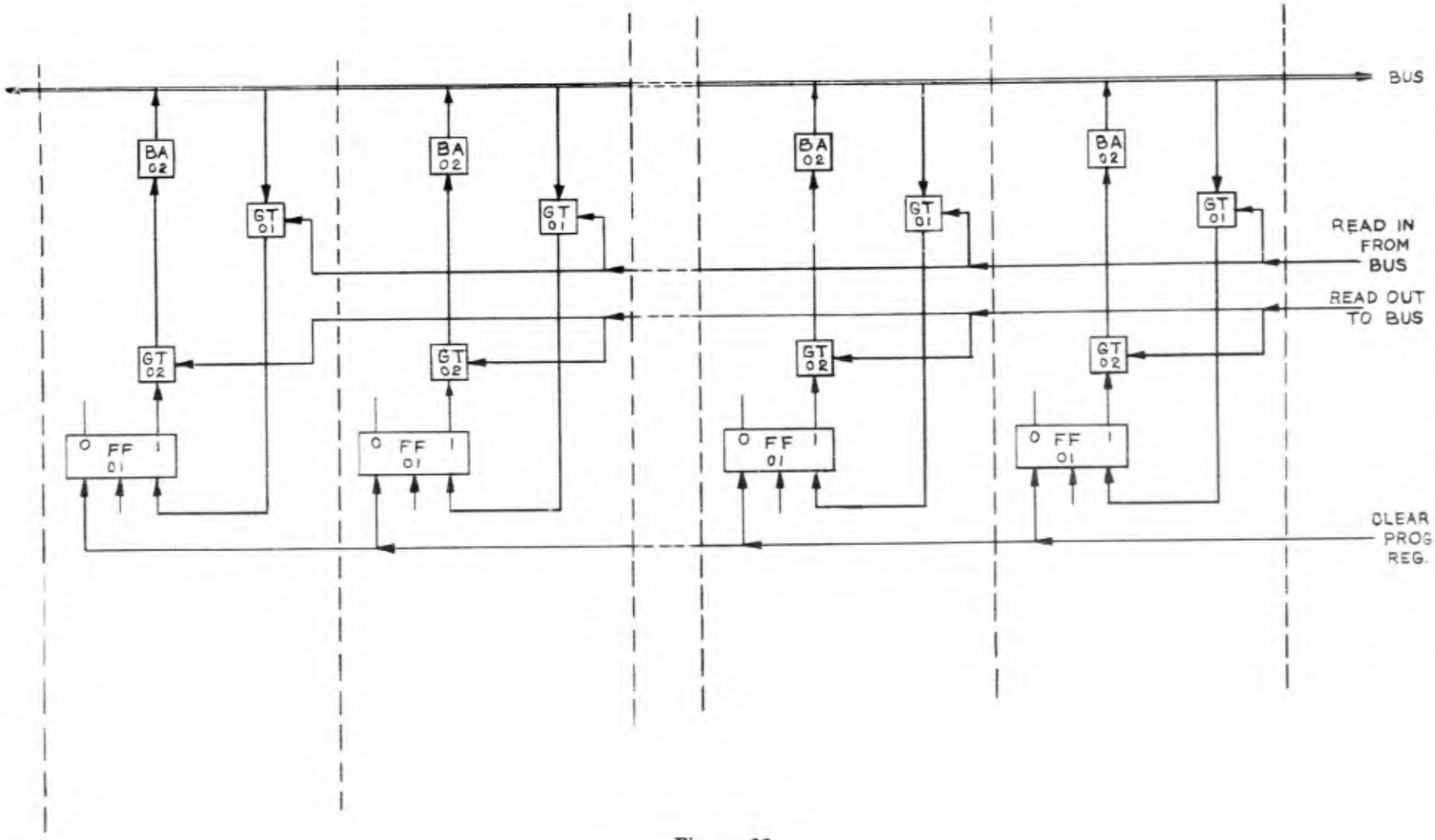

Figure 52

PROGRAM REGISTER

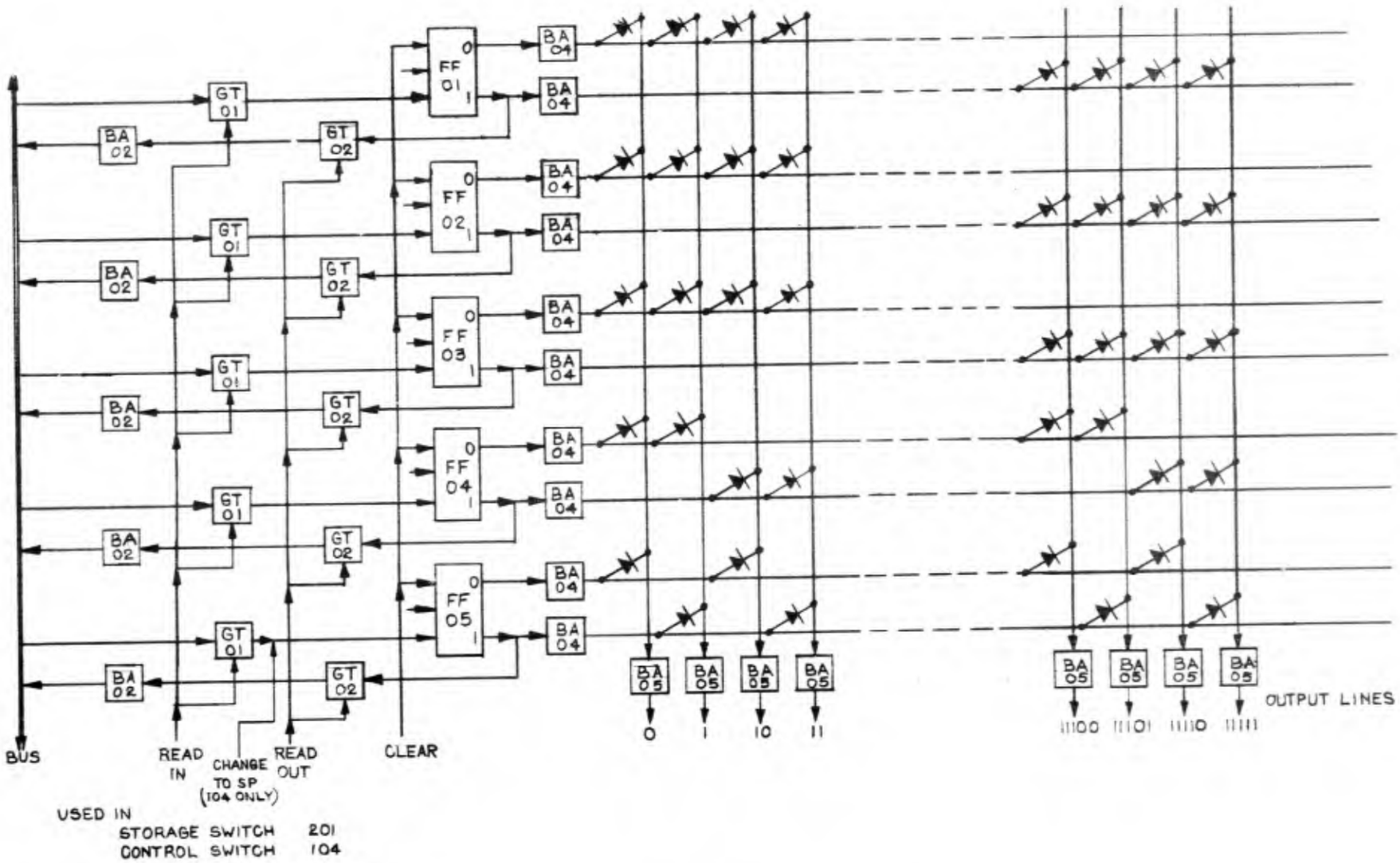

Figure 53
CONTROL SWITCH

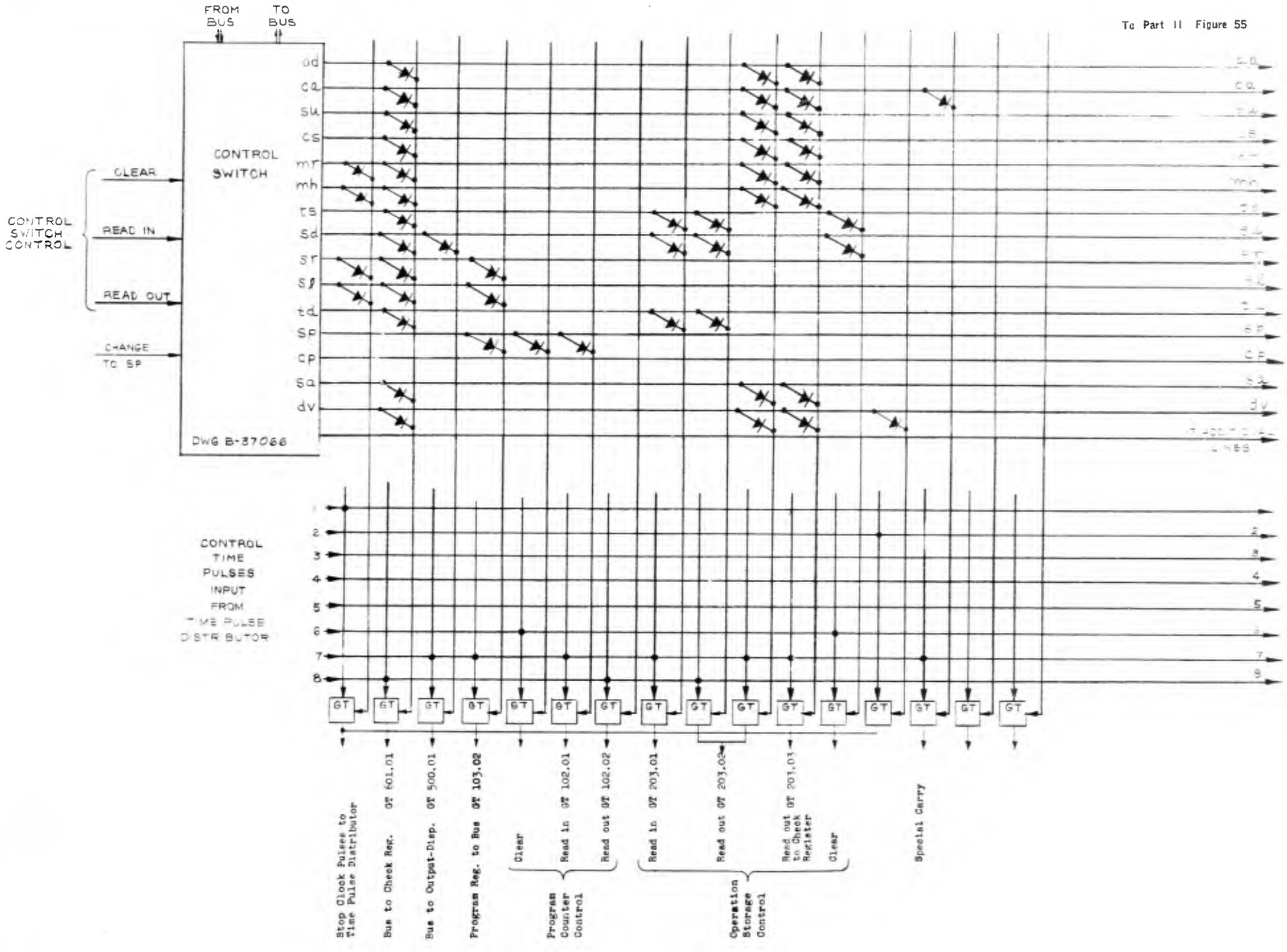

Figure 54

OPERATION MATRIX I

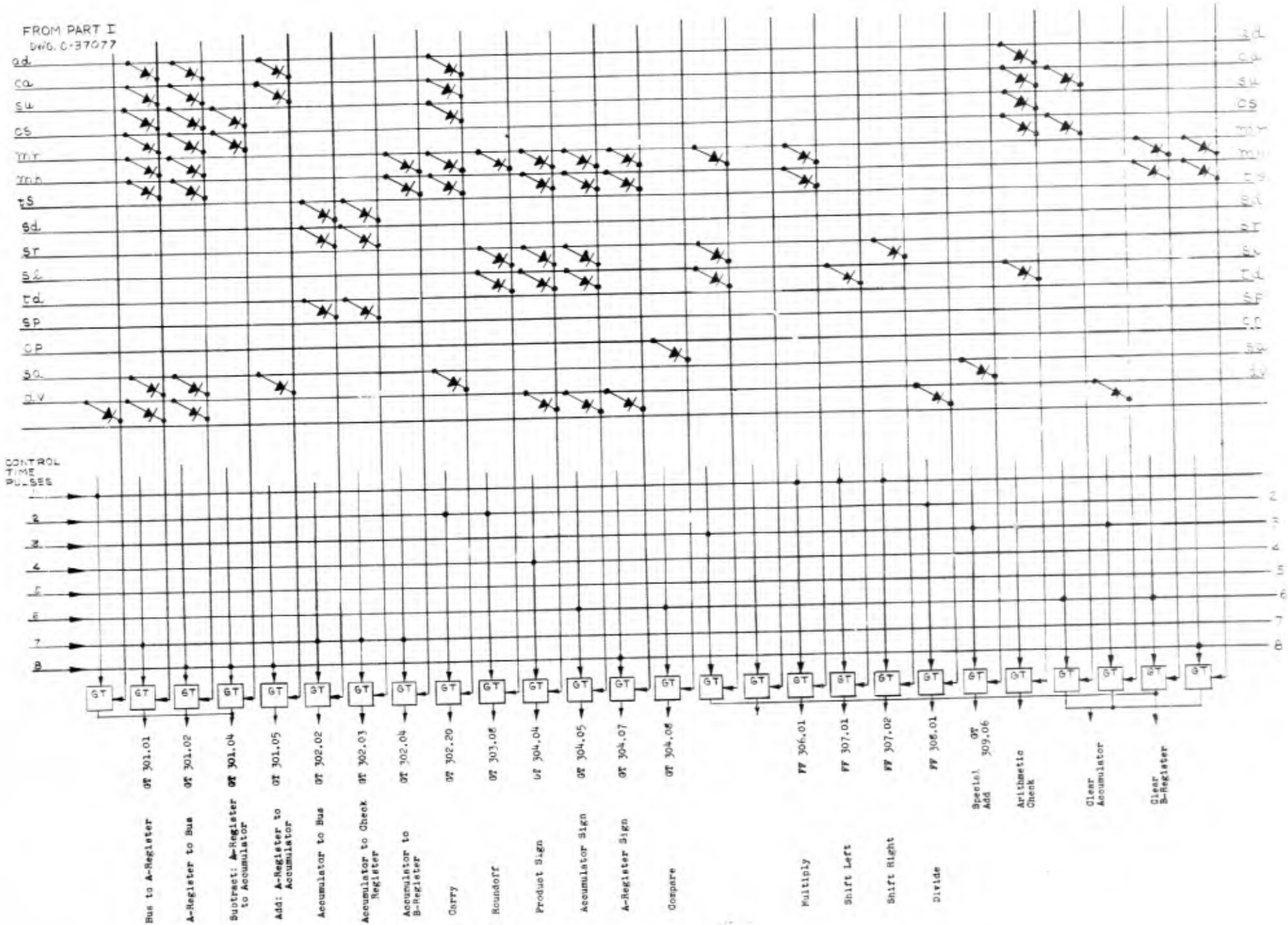

Figure 55

OPERATION MATRIX II

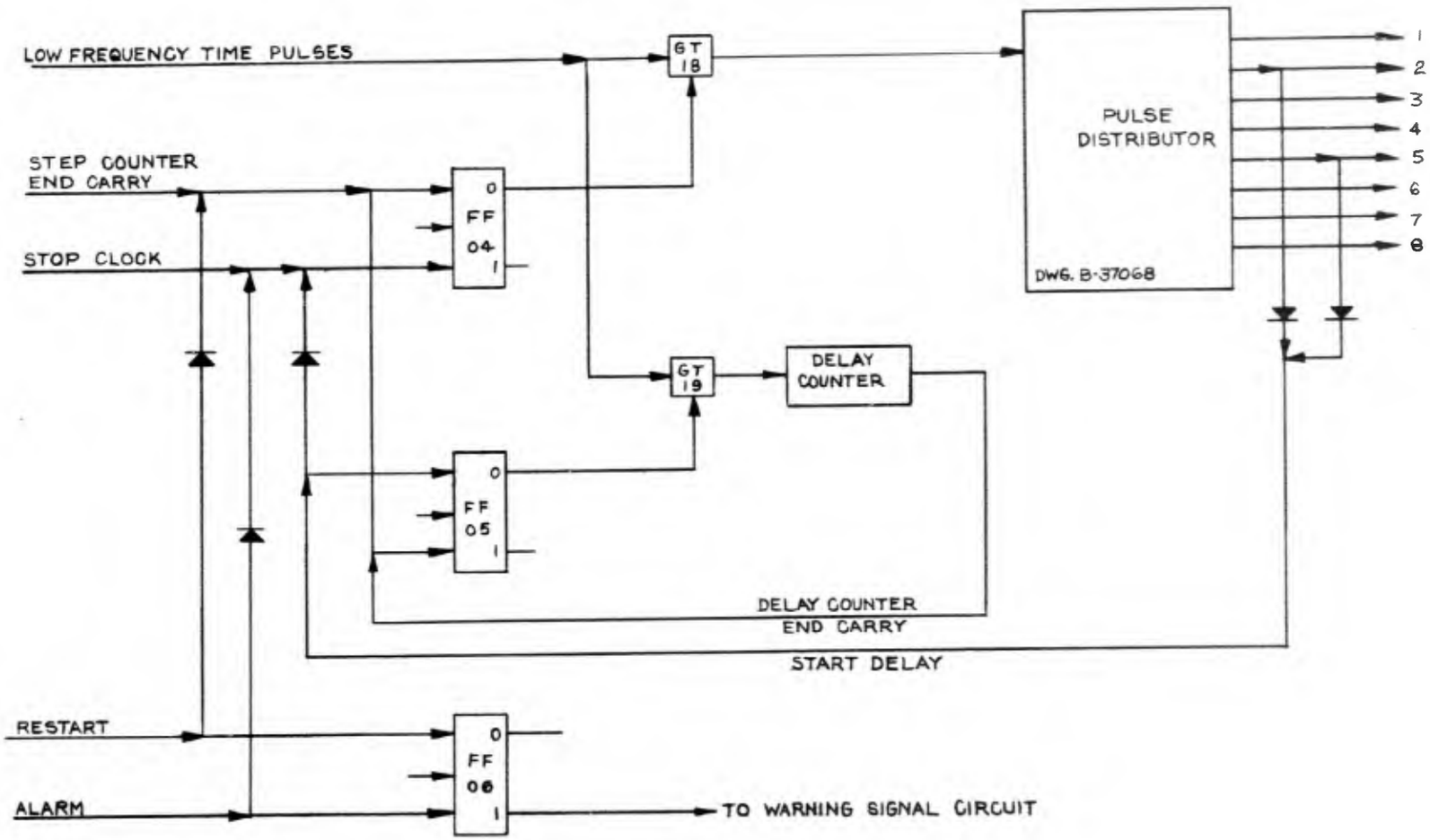

Figure 56

TIME PULSE DISTRIBUTOR CONTROL

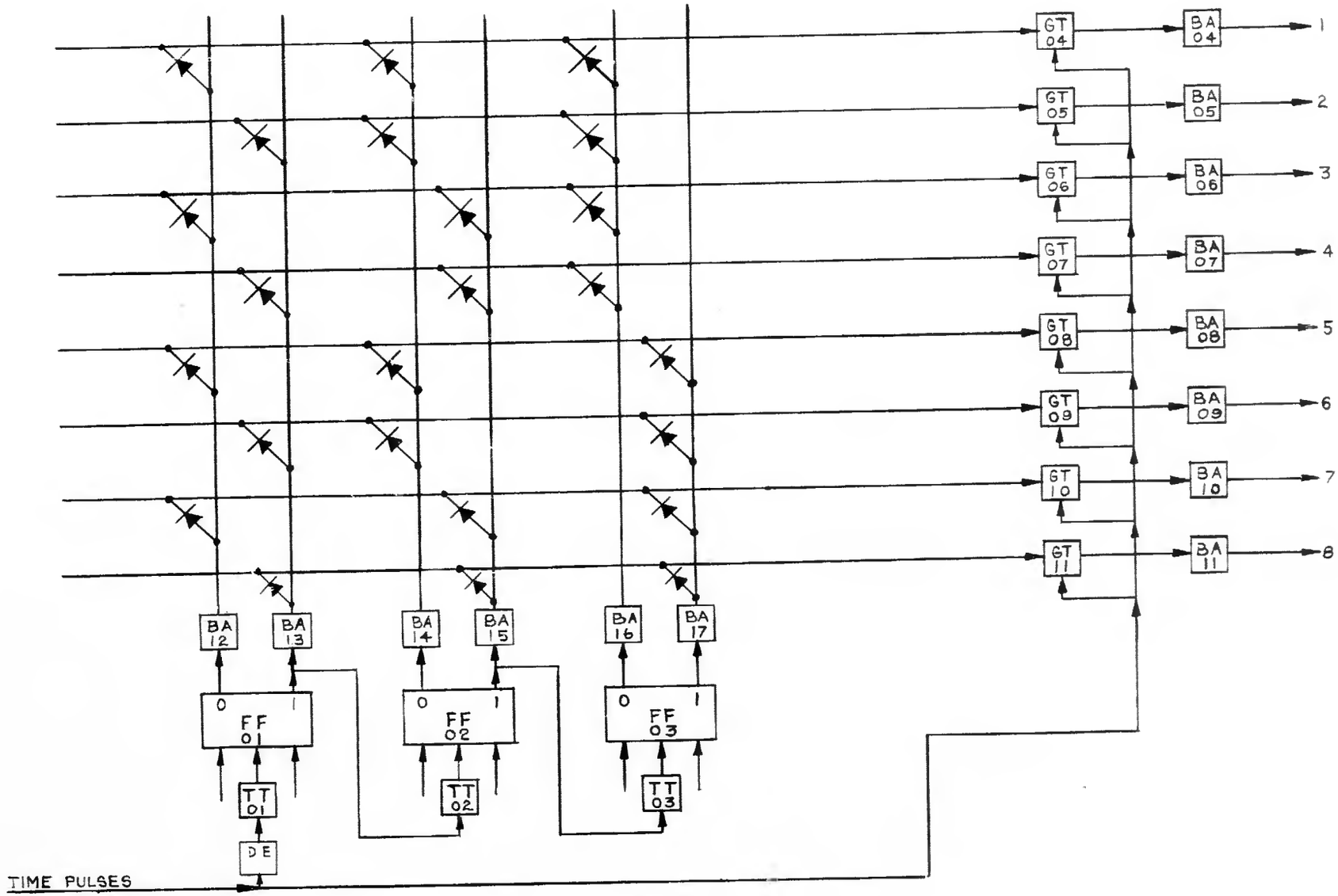

Figure 57

PULSE DISTRIBUTOR

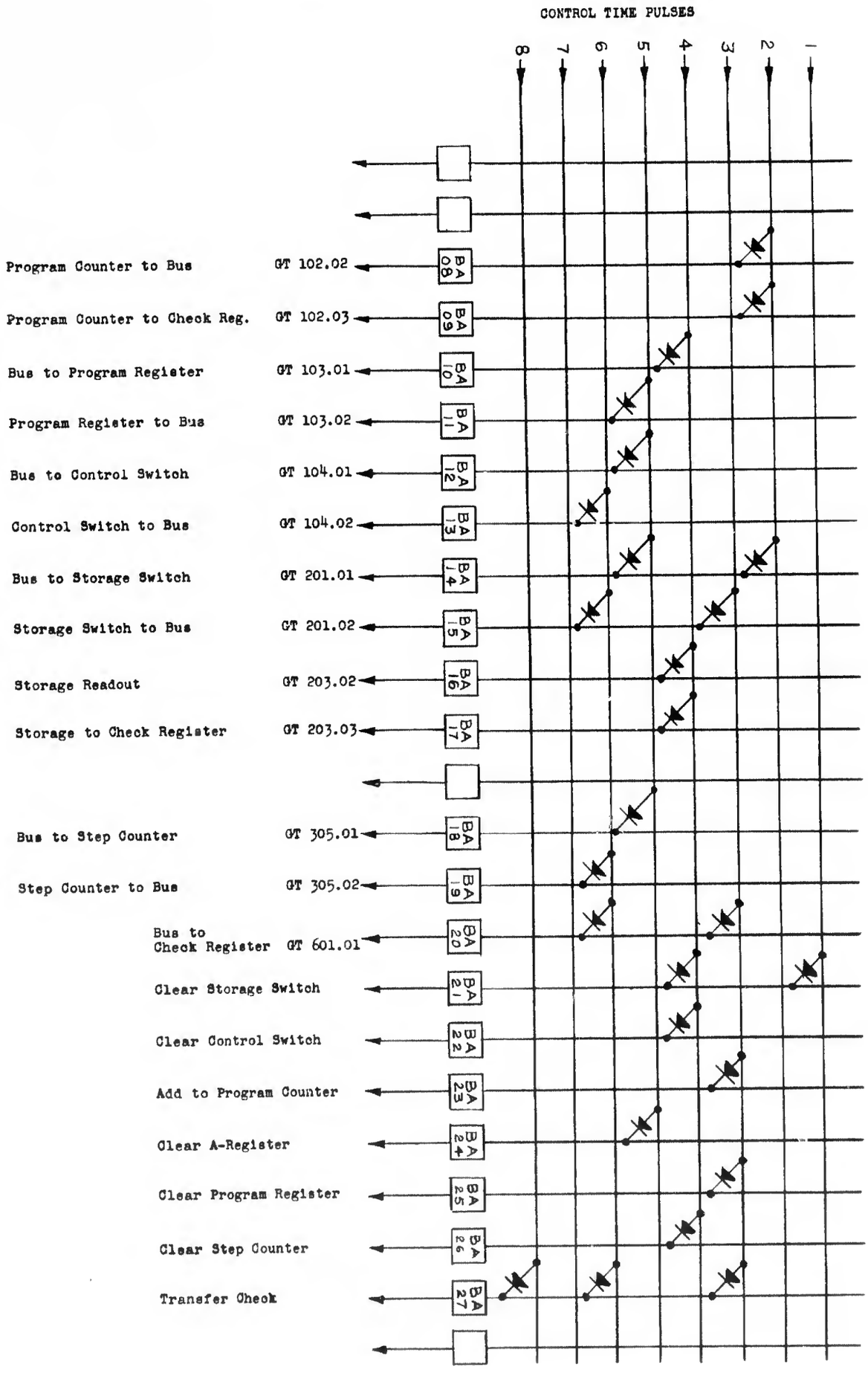

Figure 58

PROGRAM TIMING MATRIX

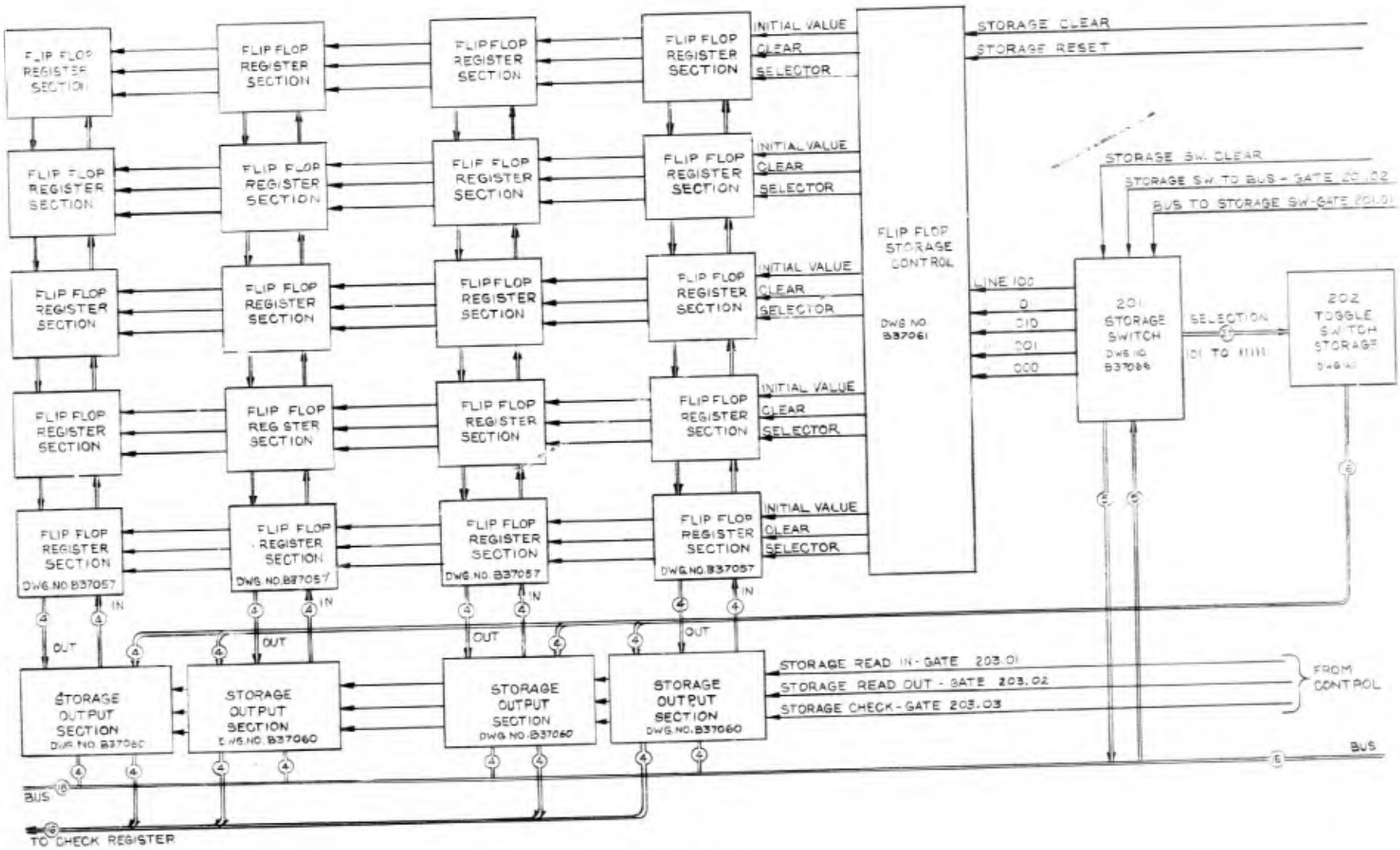

Figure 59

STORAGE CHASSIS ARRANGEMENT

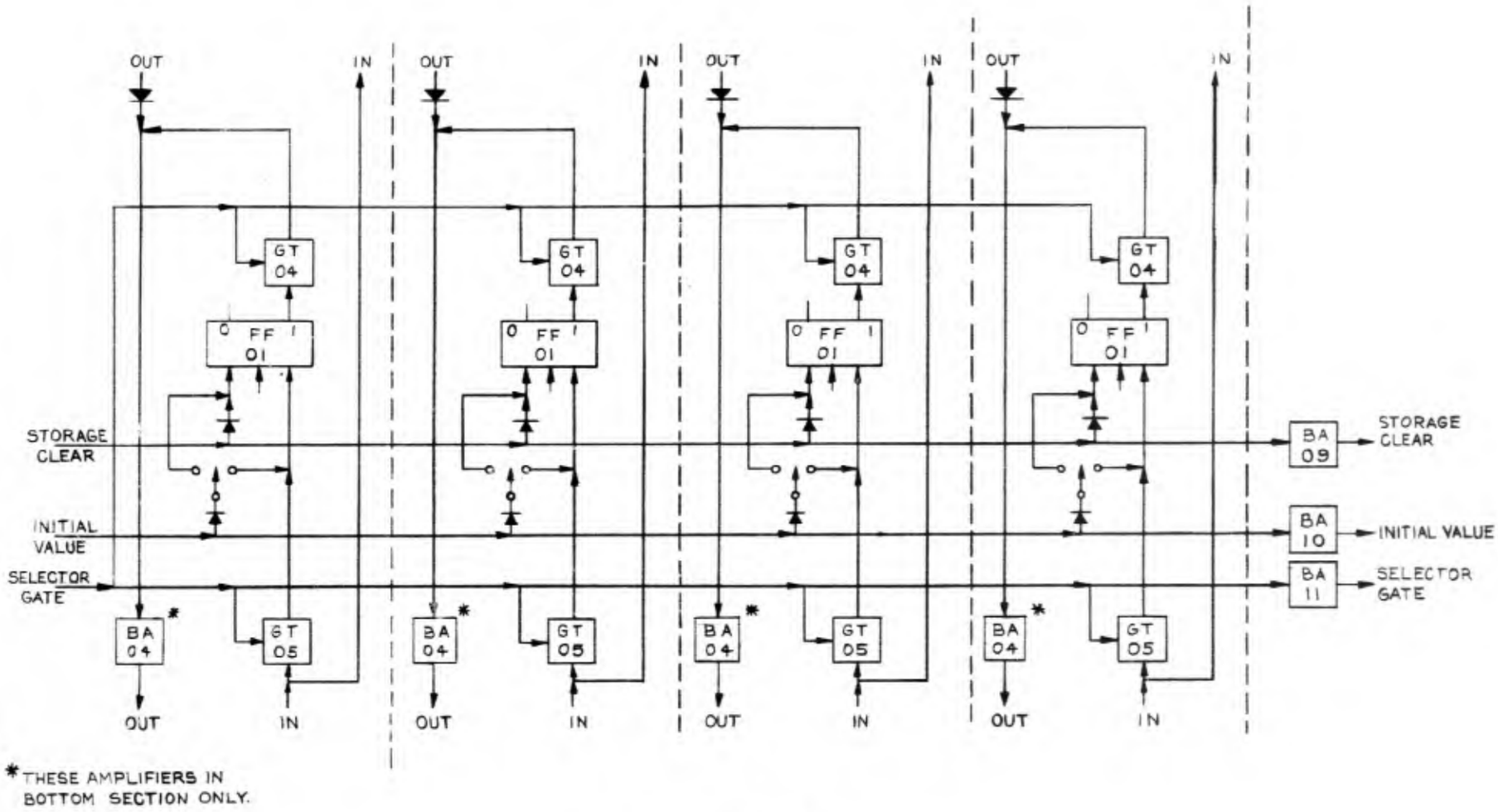

Figure 60

FLIP-FLOP STORAGE SECTION

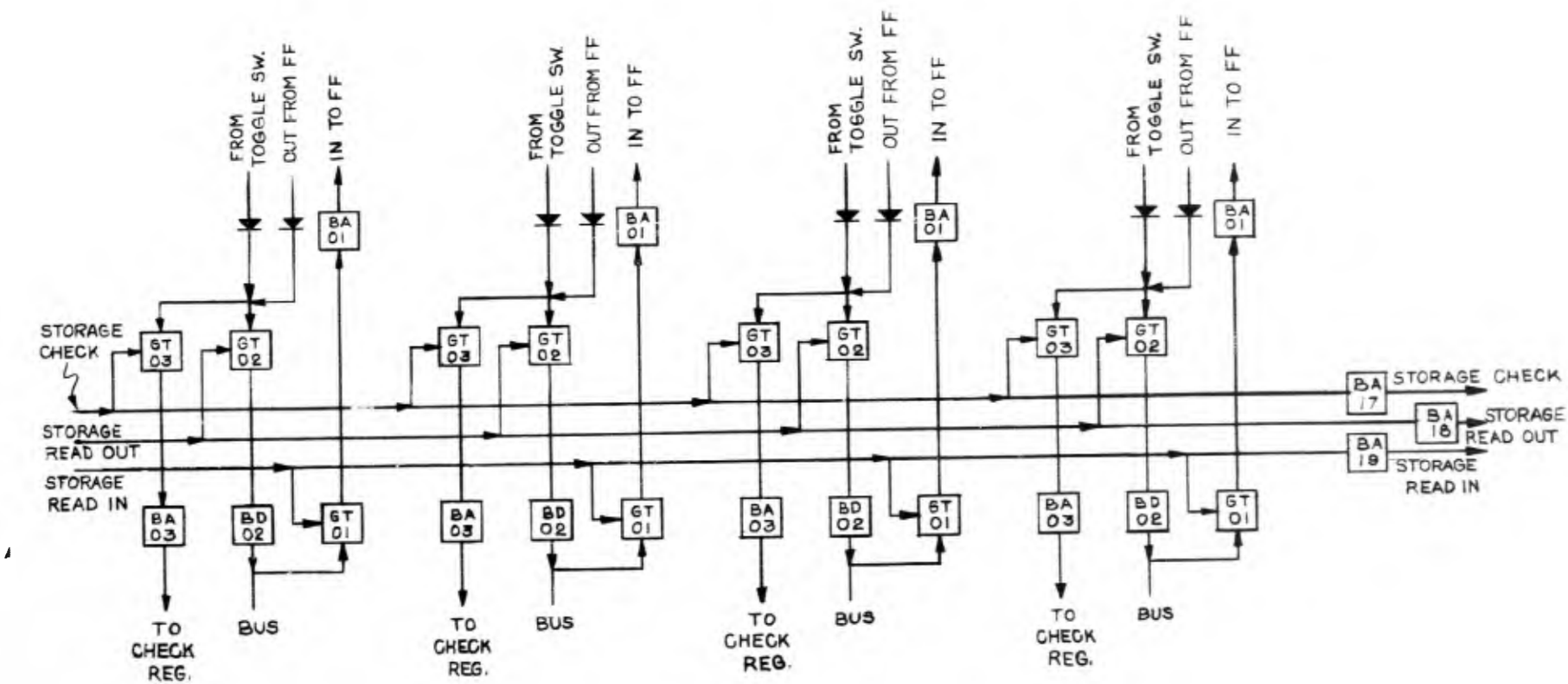

Figure 61

STORAGE OUTPUT SECTION

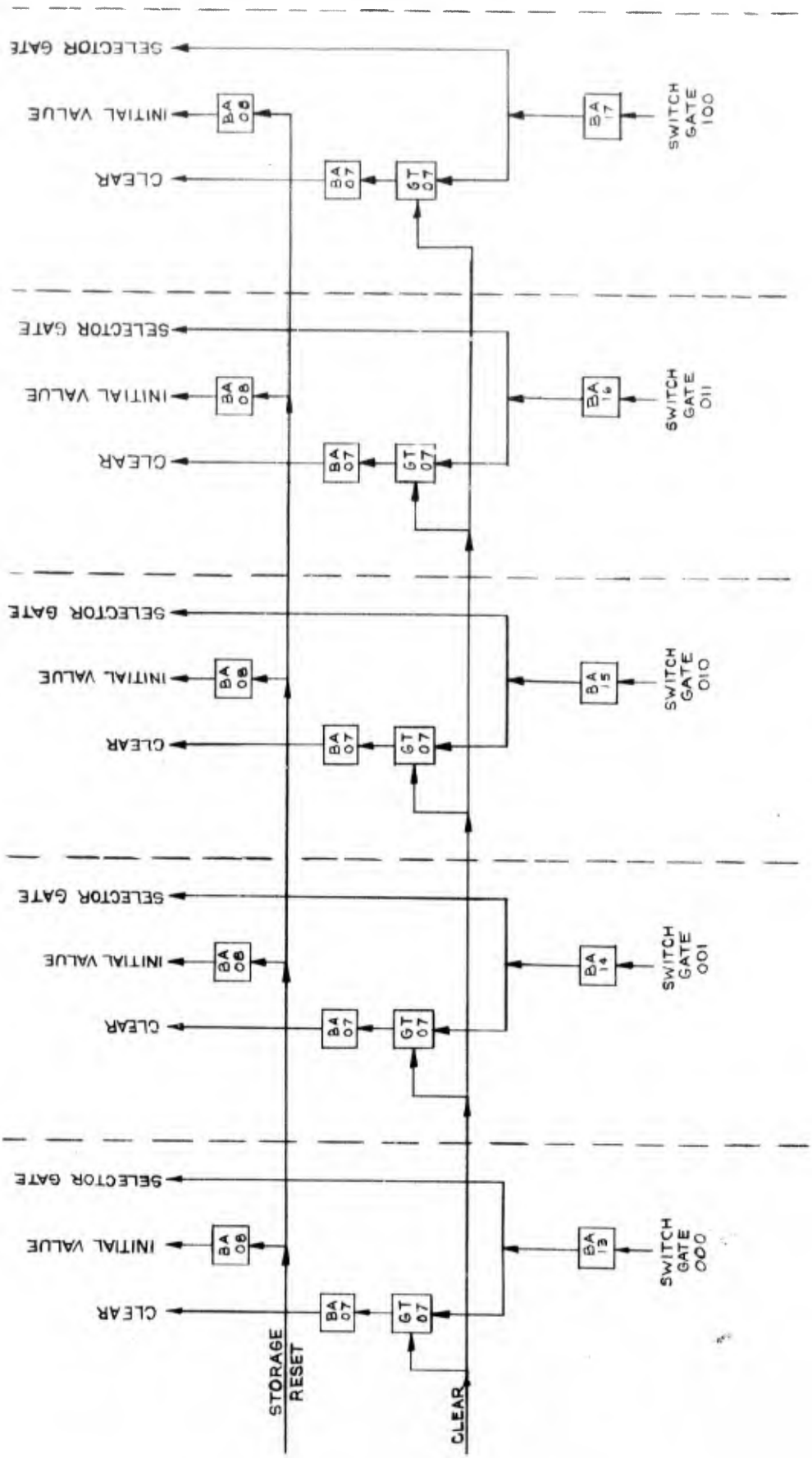

Figure 62

FLIP-FLOP STORAGE CONTROL

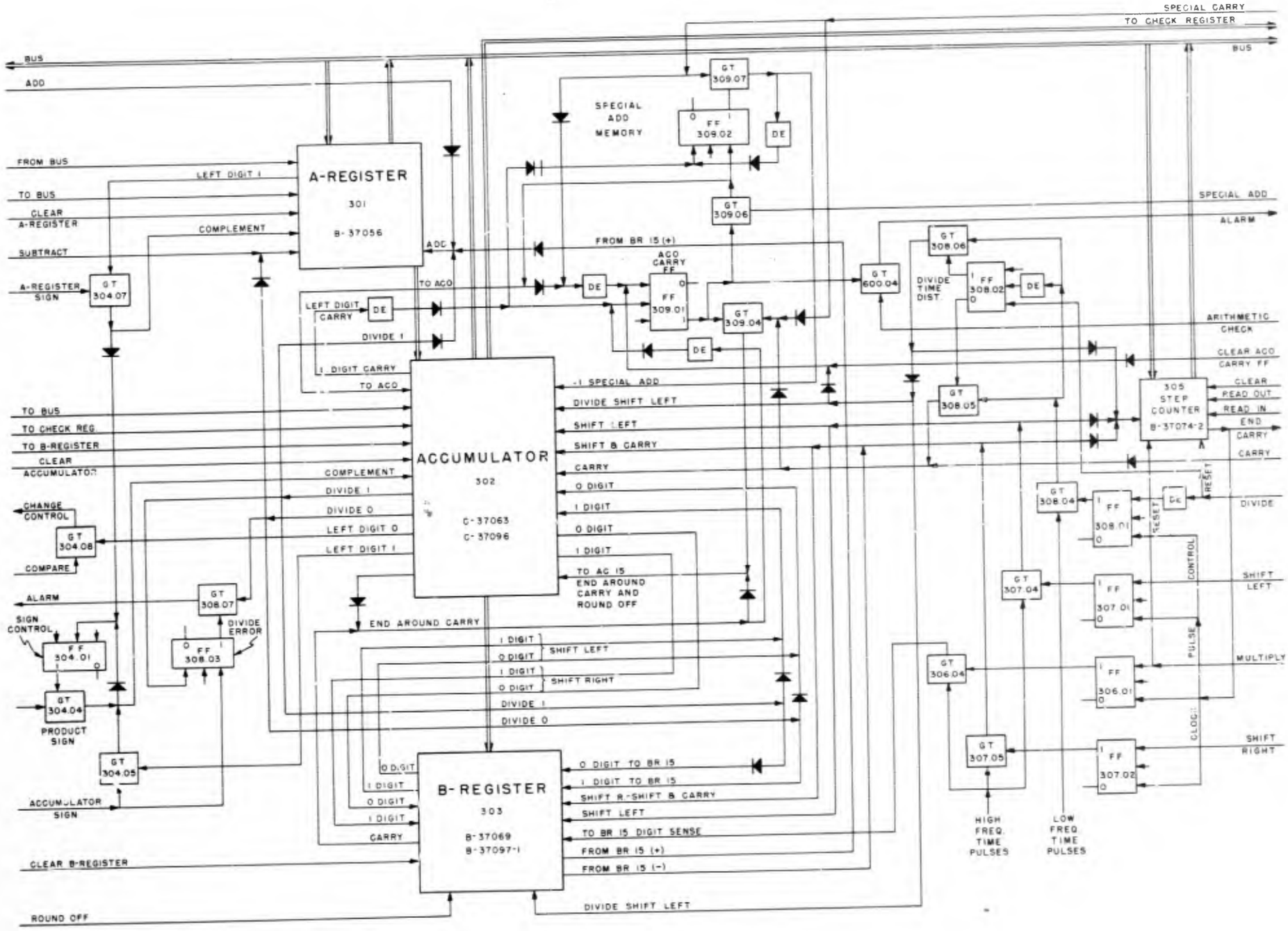

Figure 63

ARITHMETIC ELEMENT

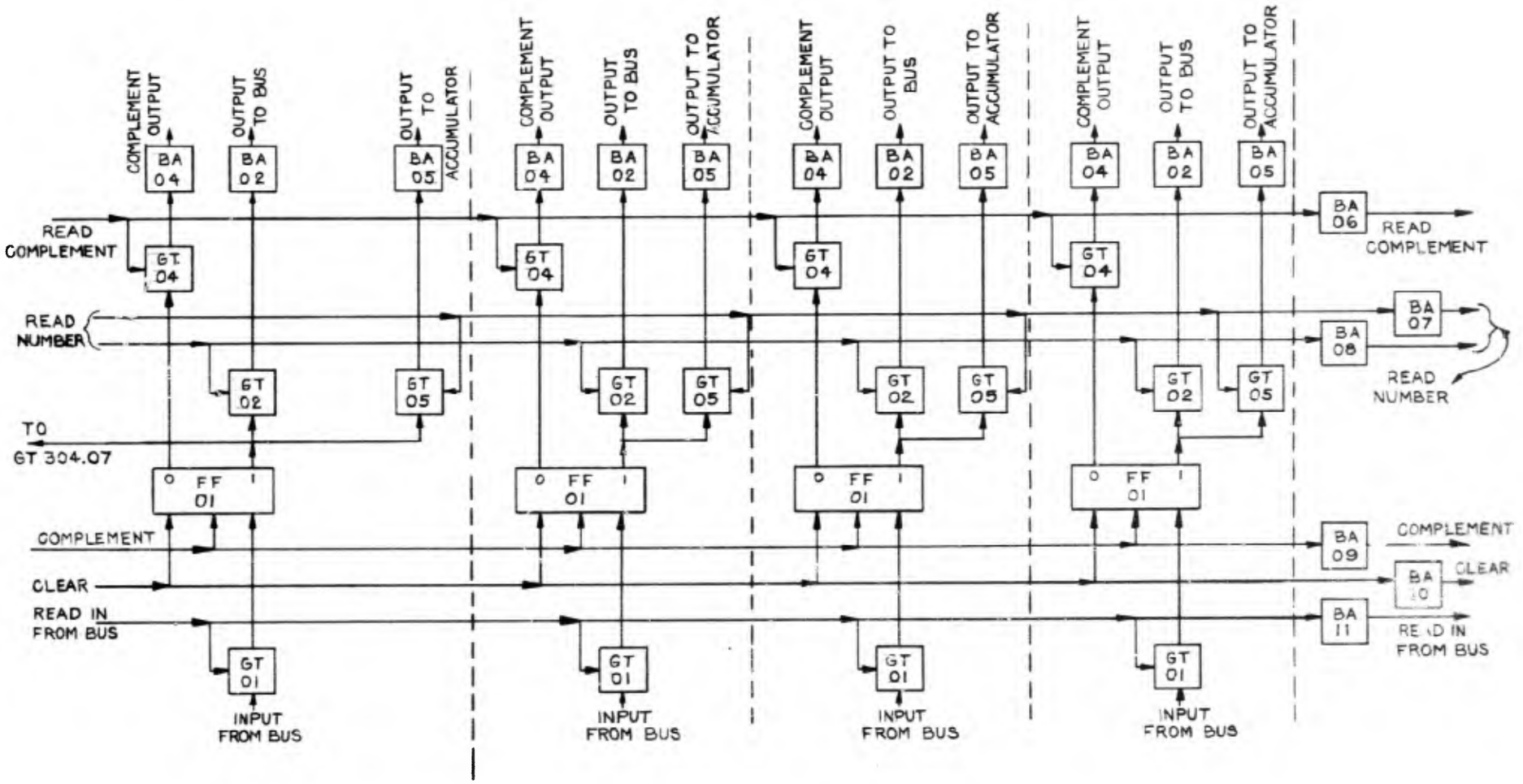

Figure 64

SECTION OF A-REGISTER

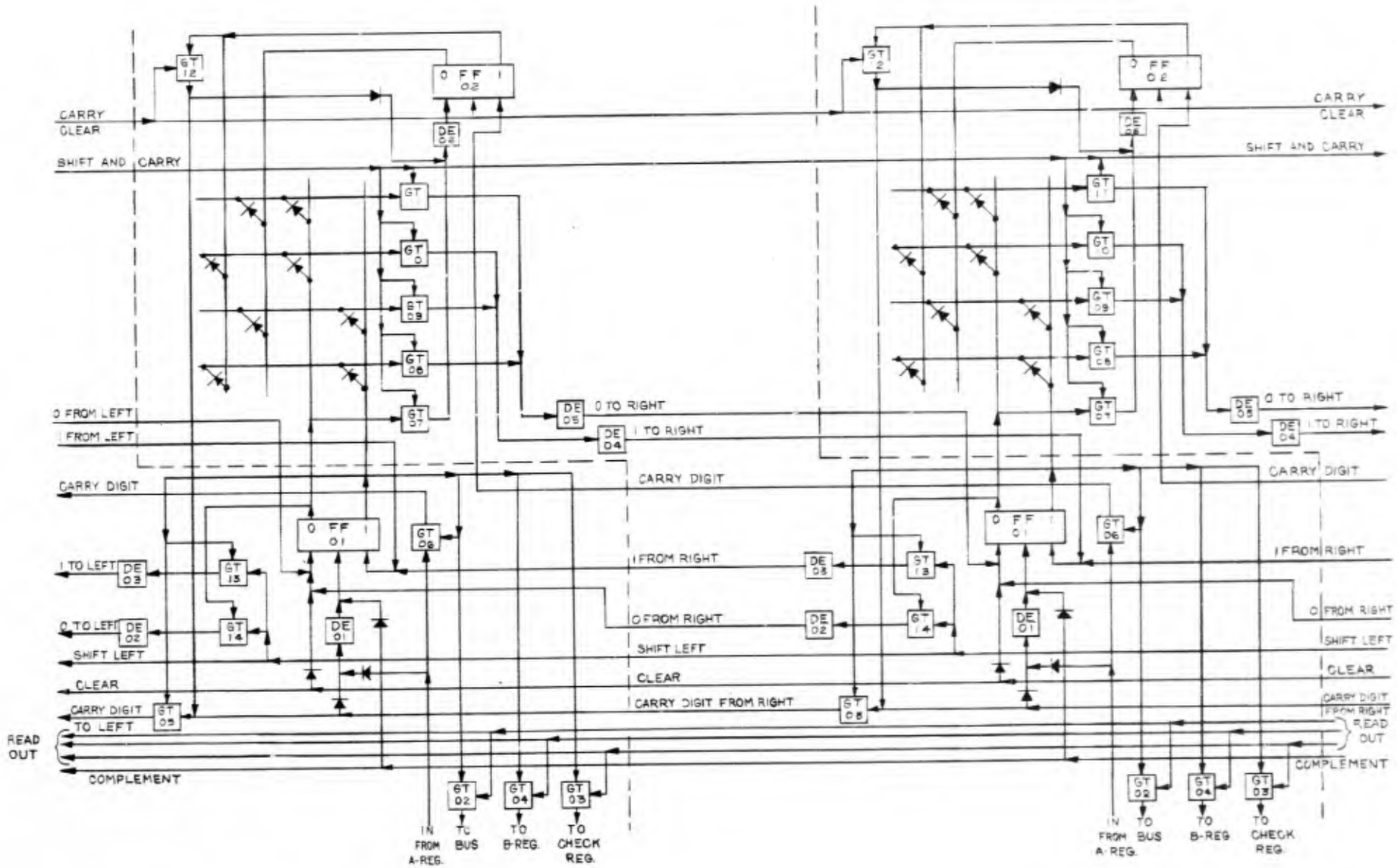

Figure 65

ACCUMULATOR SECTIONS

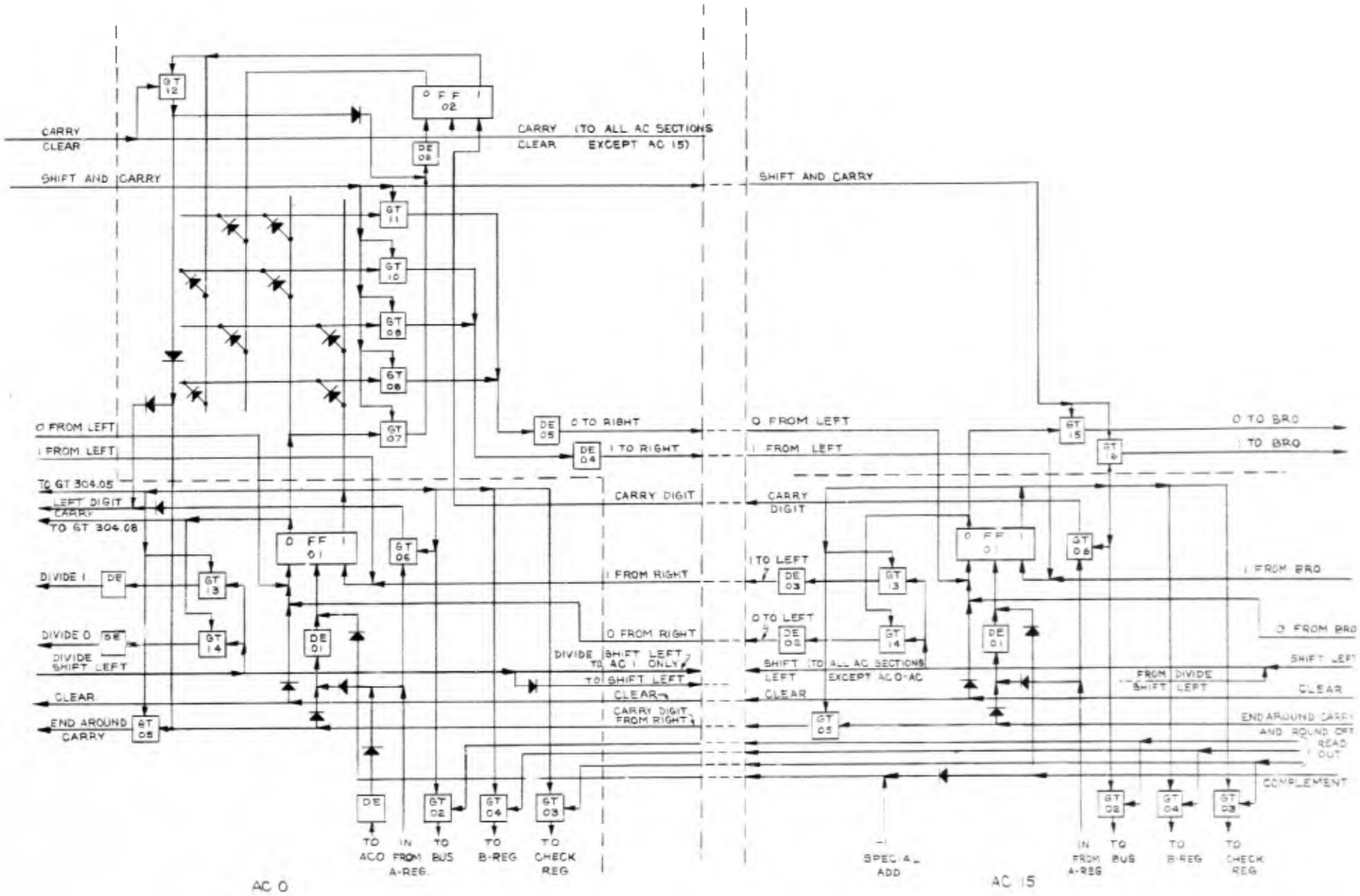

Figure 66

ACCUMULATOR SECTIONS AC0-AC15

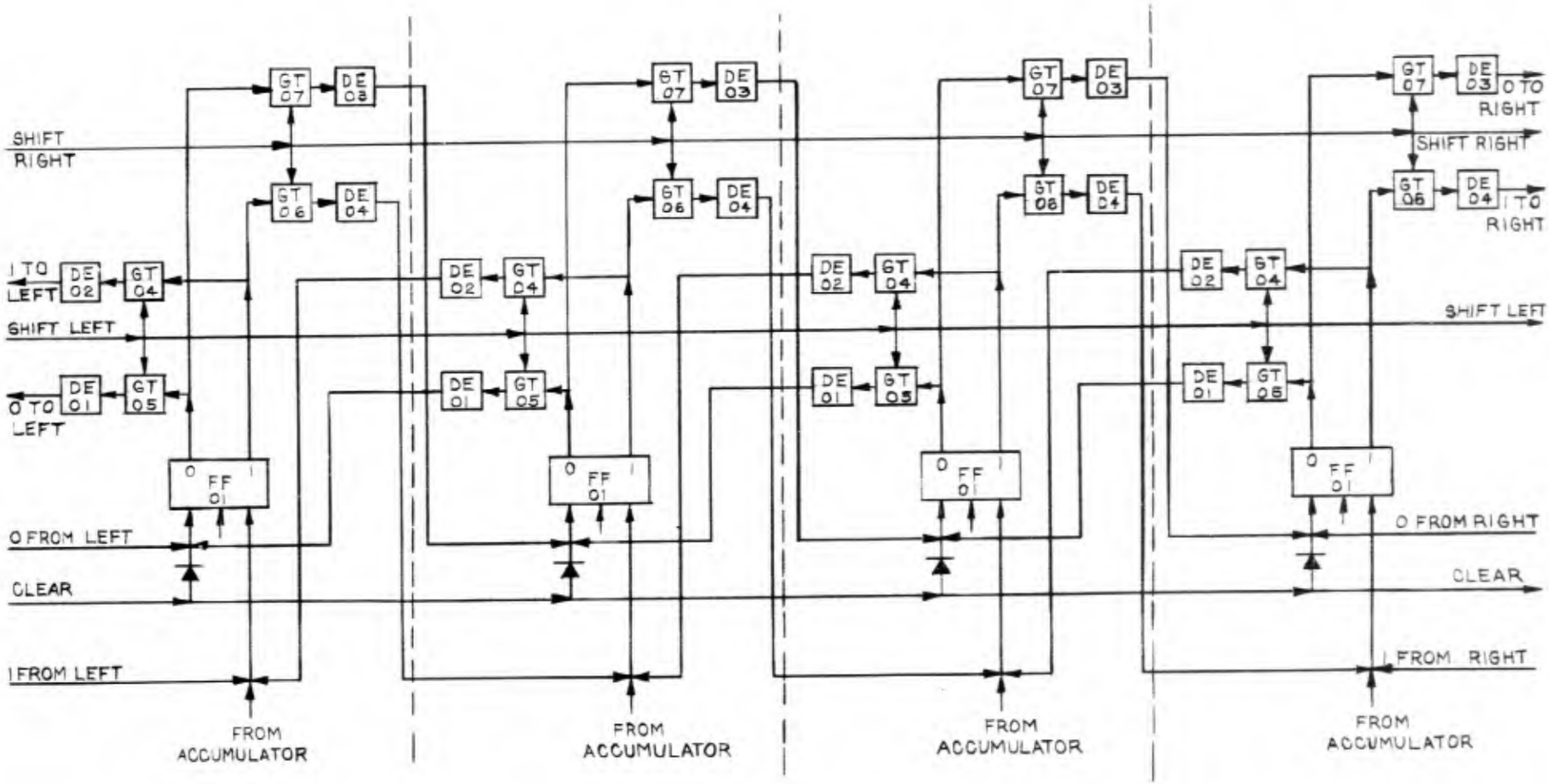

Figure 67

B-REGISTER SECTIONS

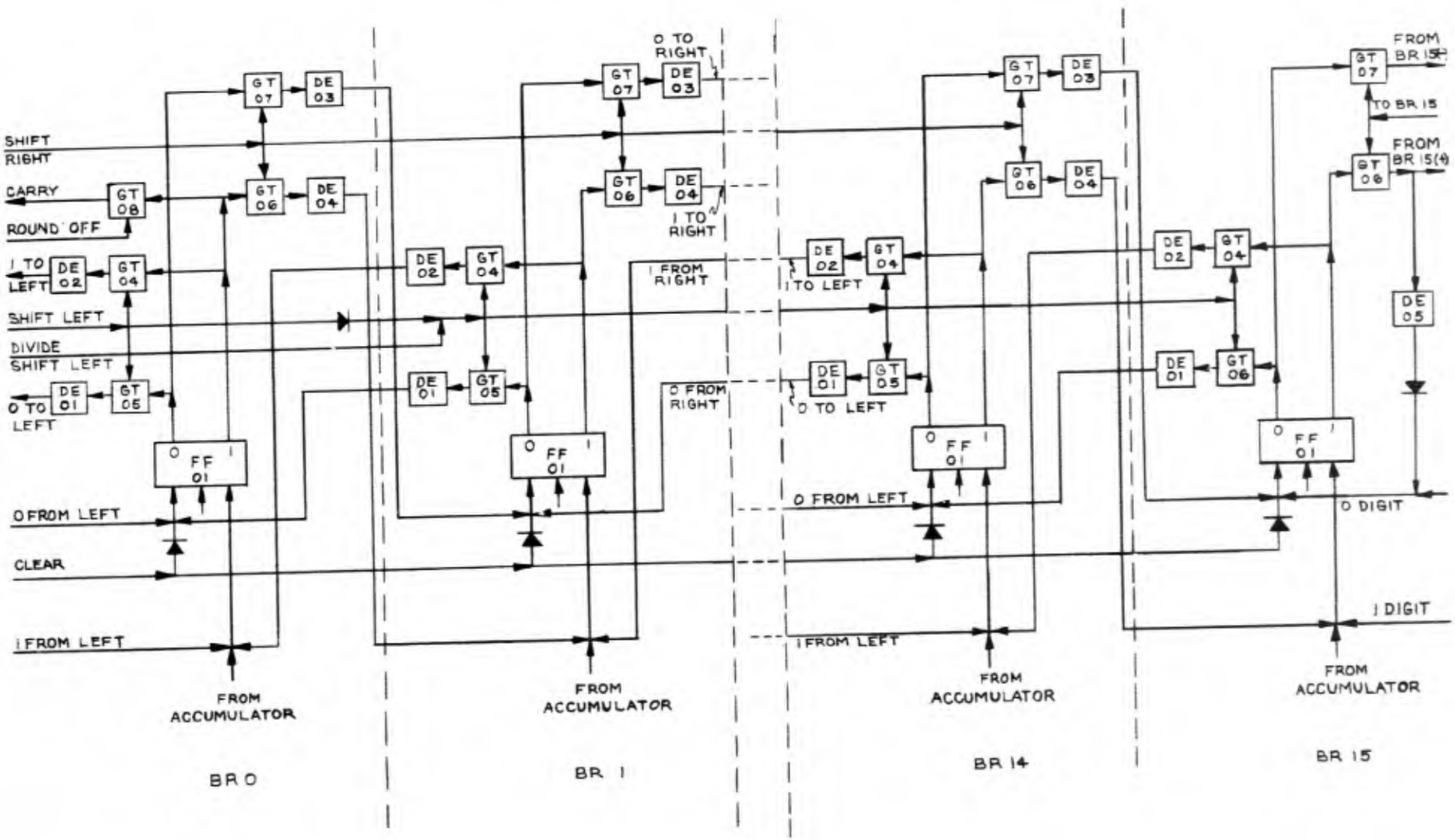

Figure 68

B-REGISTER SECTIONS BR 0, 1, 14, 15

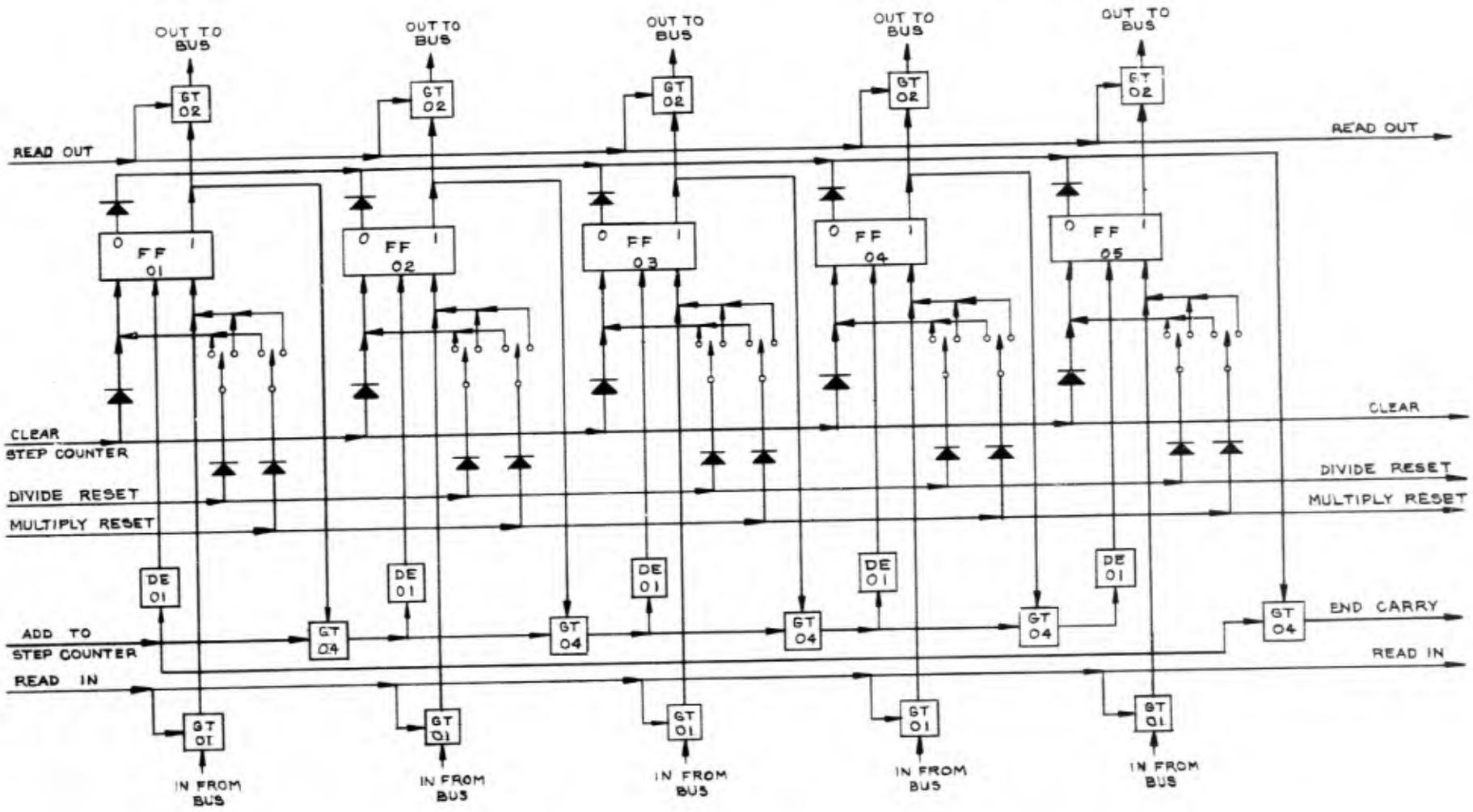

Figure 69

STEP COUNTER

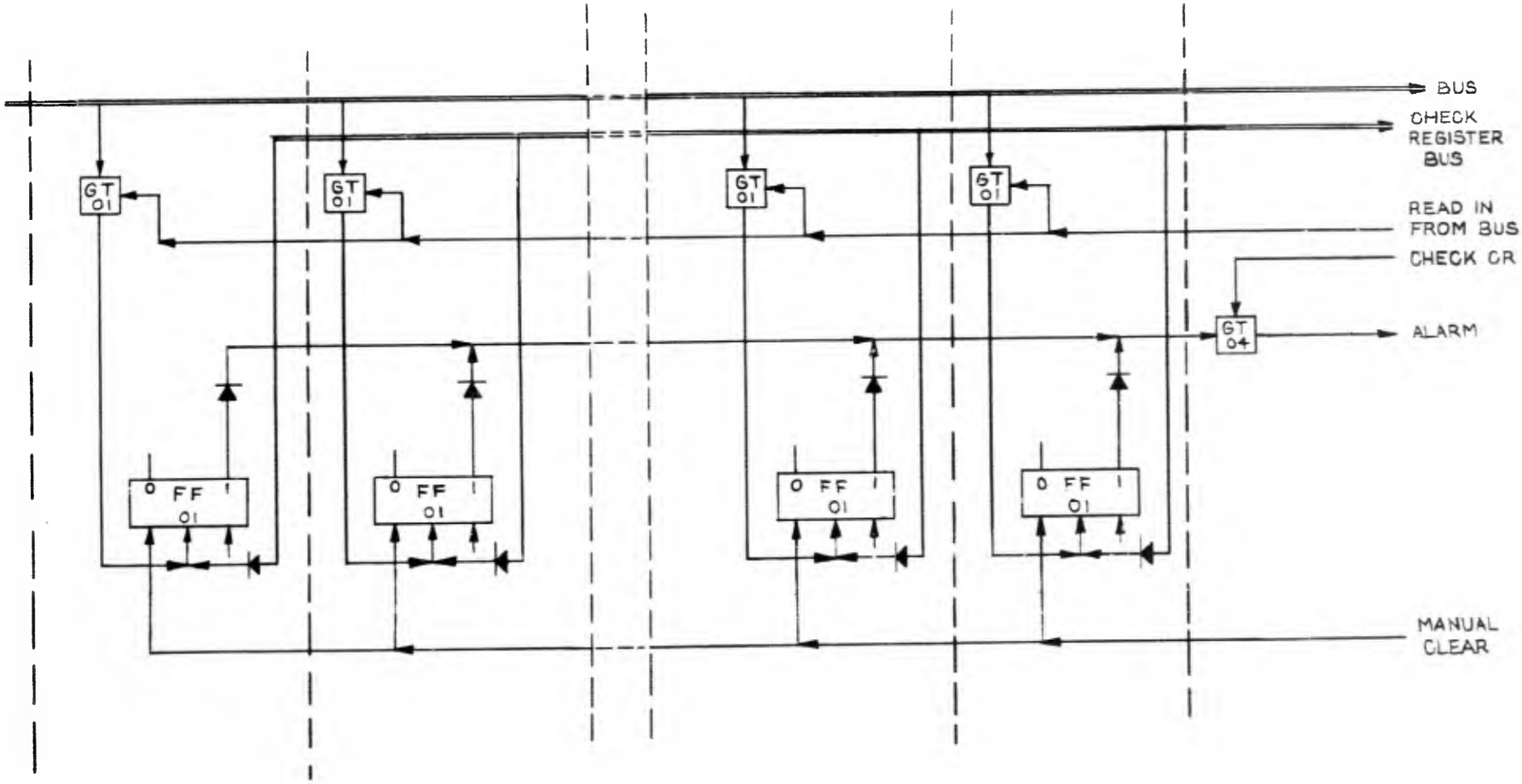

Figure 70

CHECK REGISTER

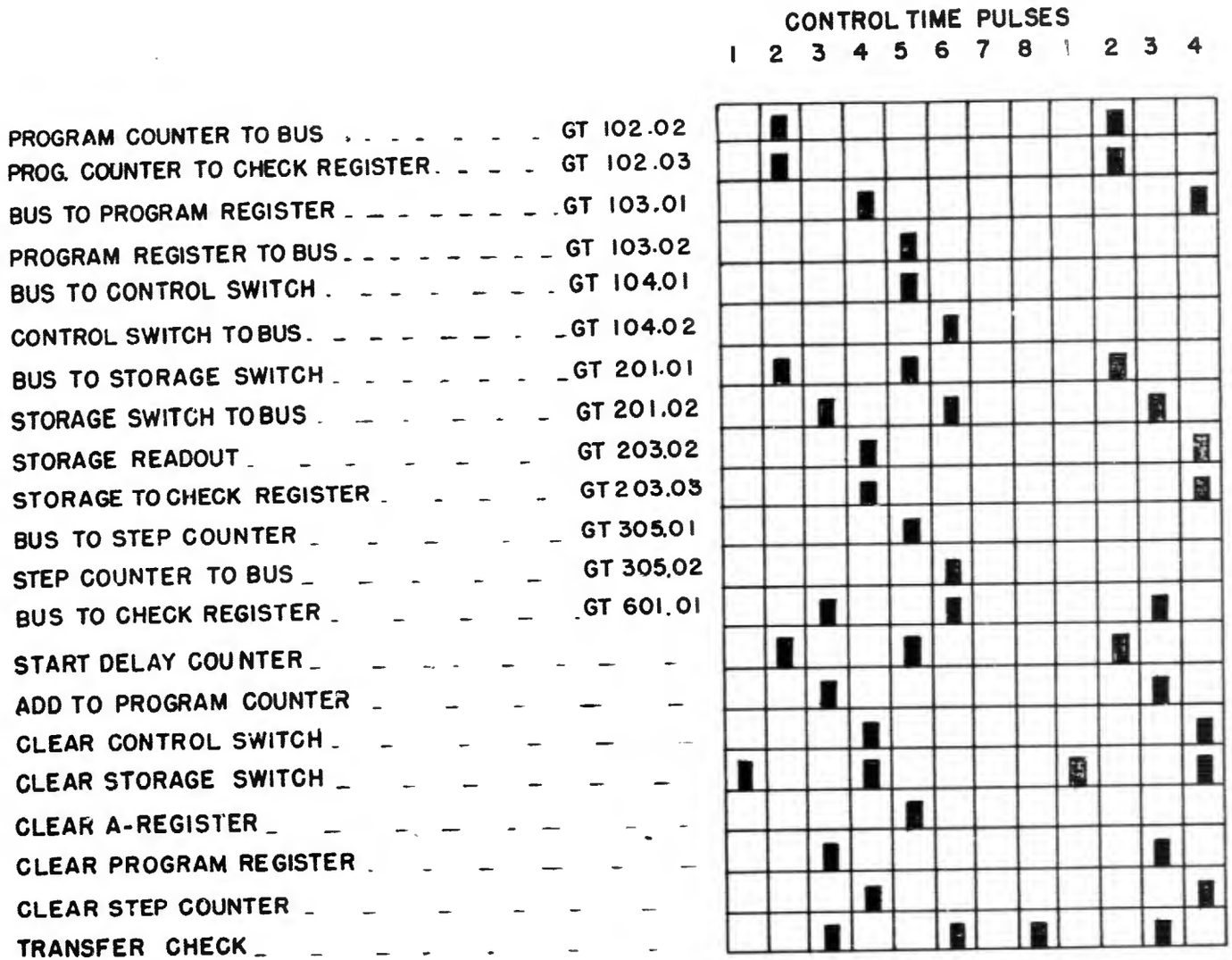

Figure 71

PROGRAM TIMING

OPERATION: ADD ad

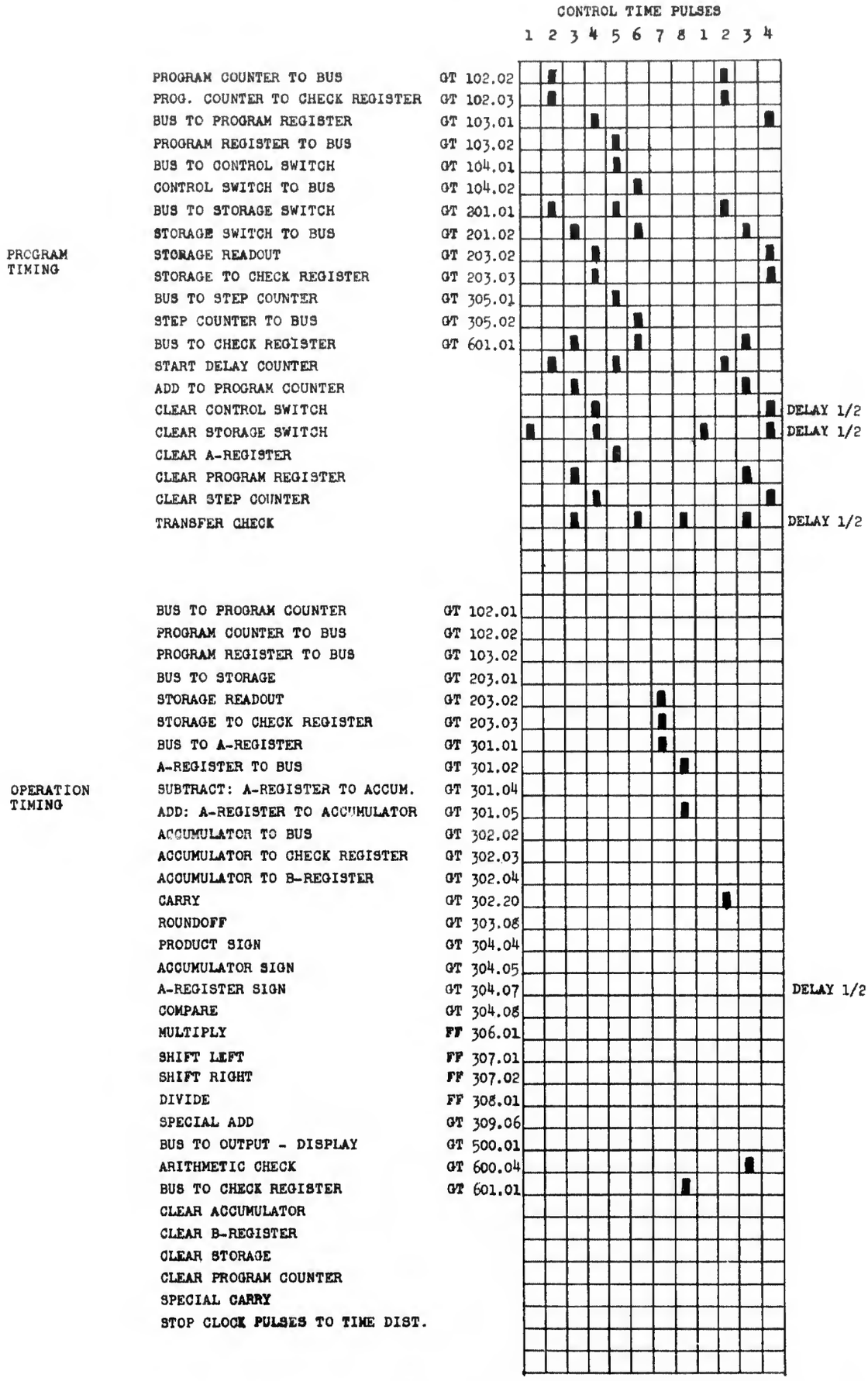

Figure 72

TIMING FOR ADD

OPERATION: CLEAR AND ADD ca

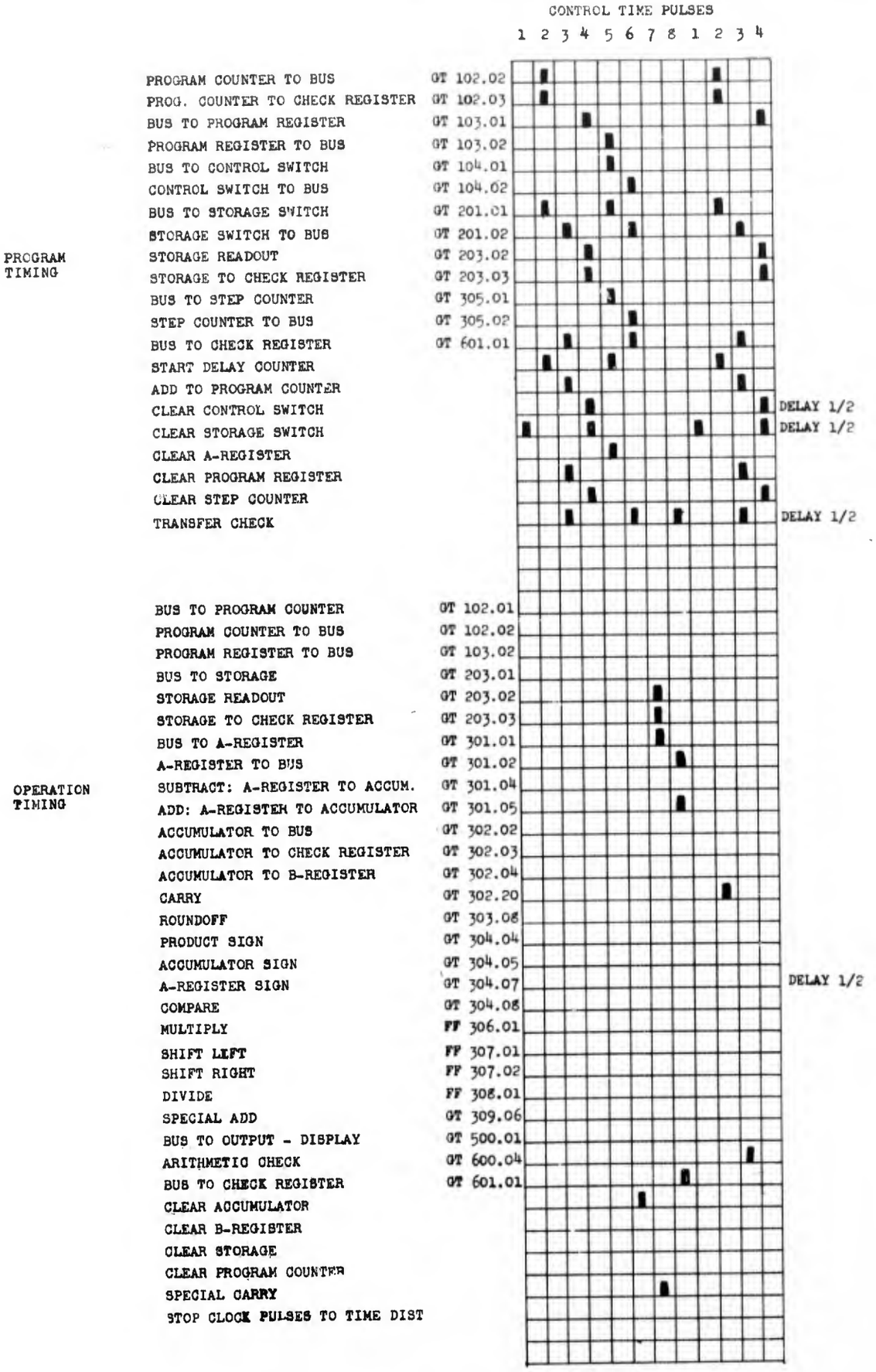

Figure 73

TIMING FOR CLEAR AND ADD

OPERATION: SUBTRACT su

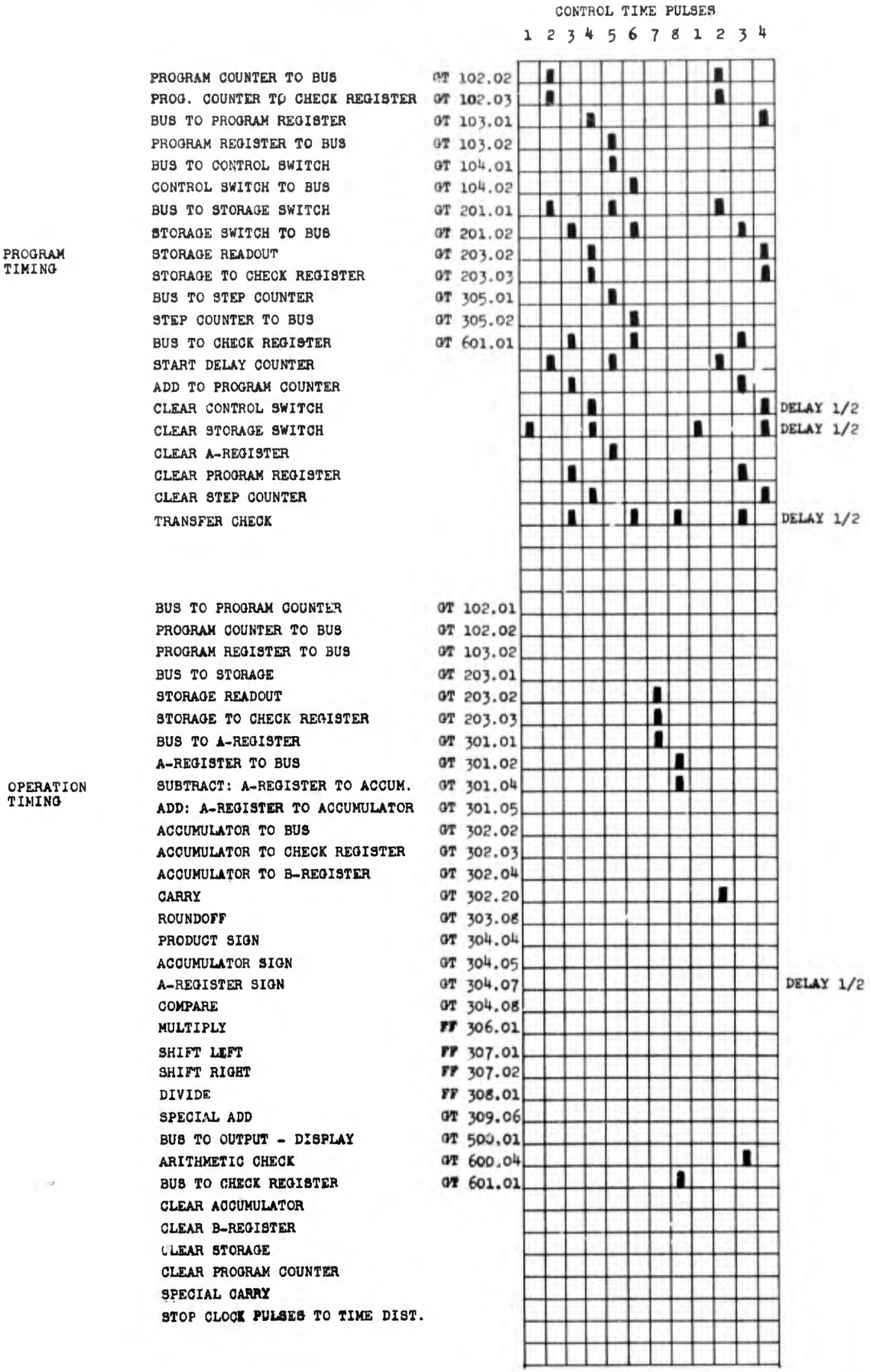

Figure 74

TIMING FOR SUBTRACT

OPERATION: CLEAR AND SUBTRACT cs

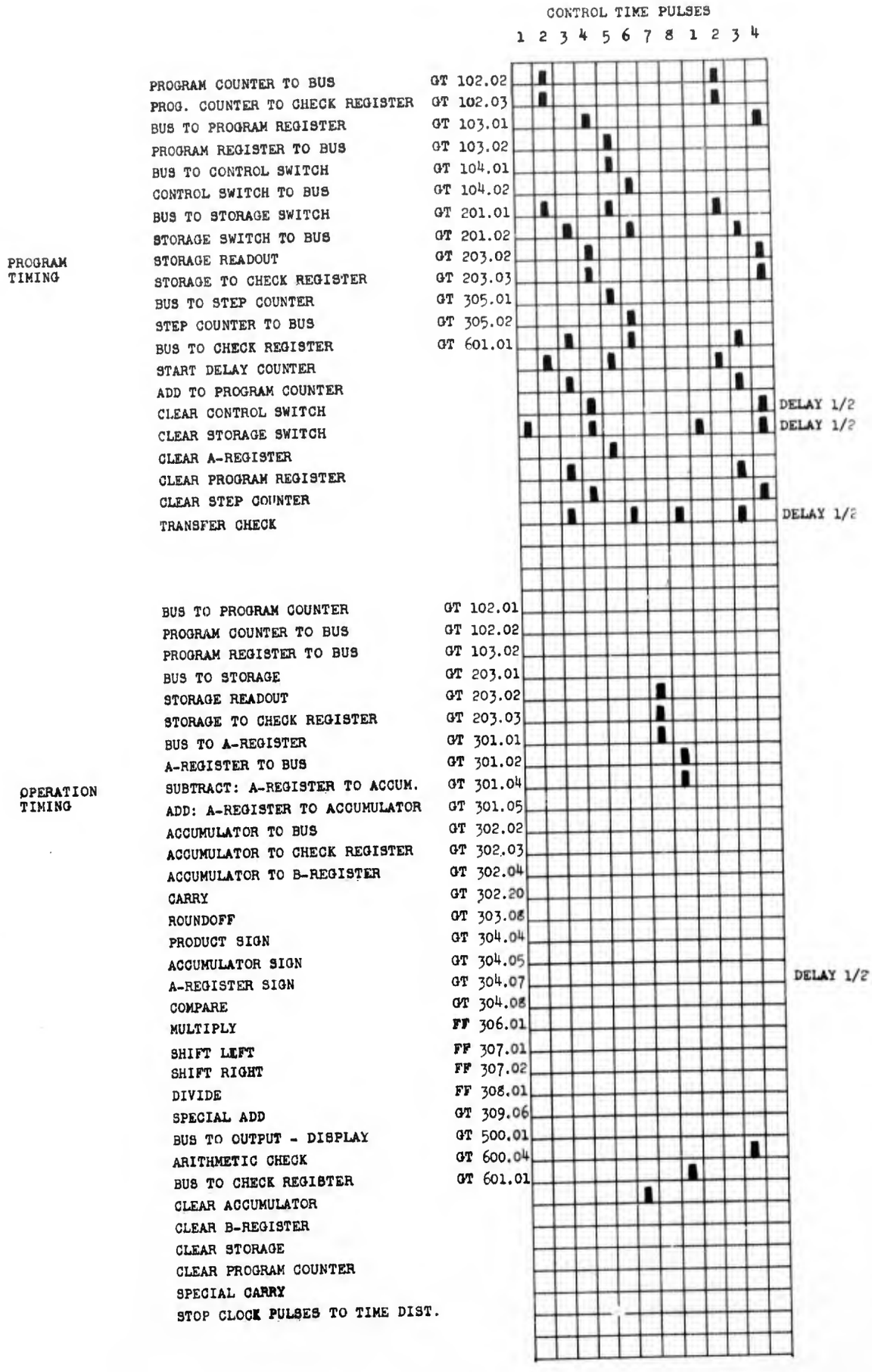

Figure 75

TIMING FOR CLEAR AND SUBTRACT

OPERATION: MULTIPLY AND ROUNDOFF mr

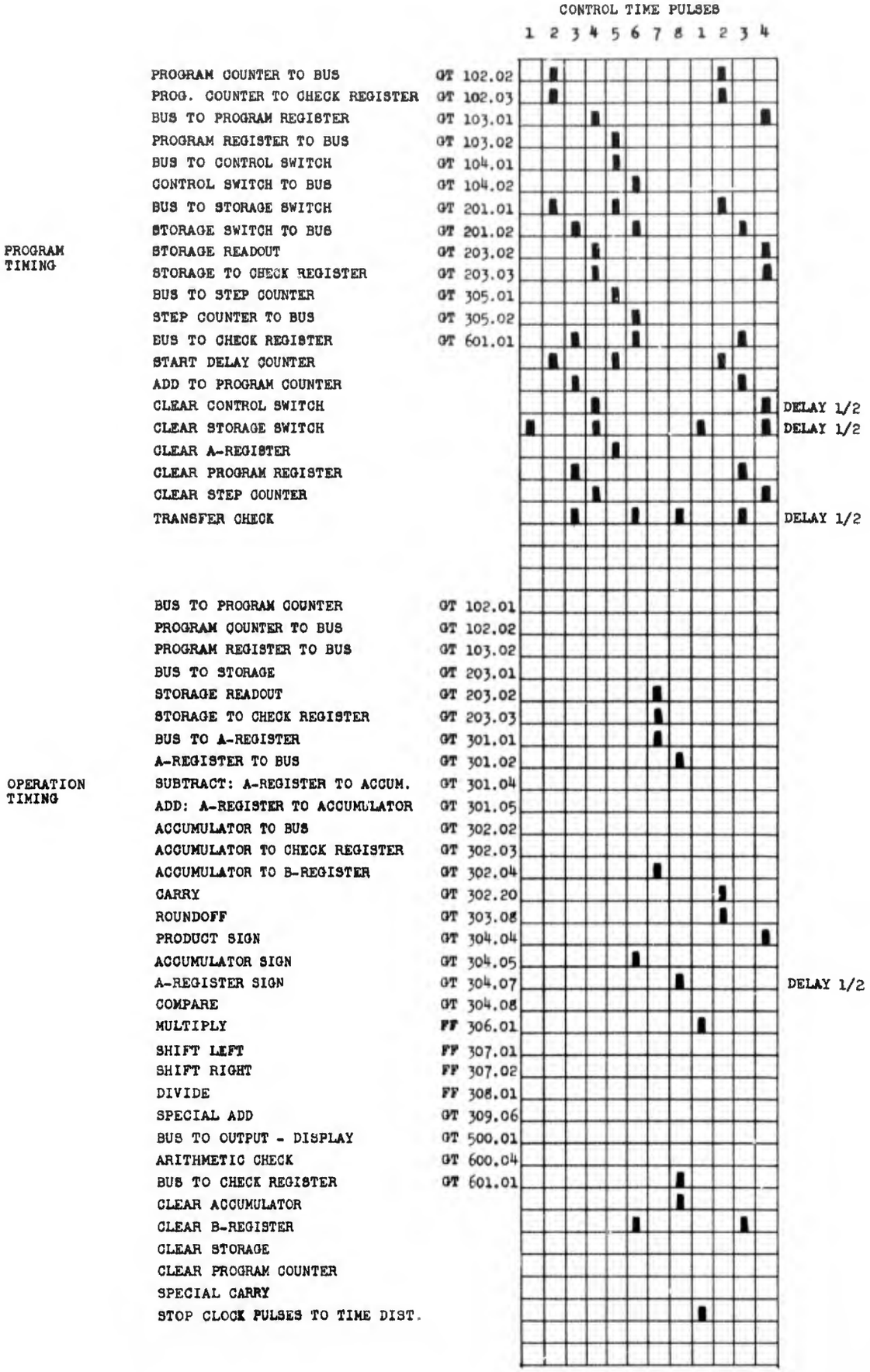

Figure 76

TIMING FOR MULTIPLY AND ROUNDOFF

OPERATION: MULTIPLY AND HOLD FULL PRODUCT mh

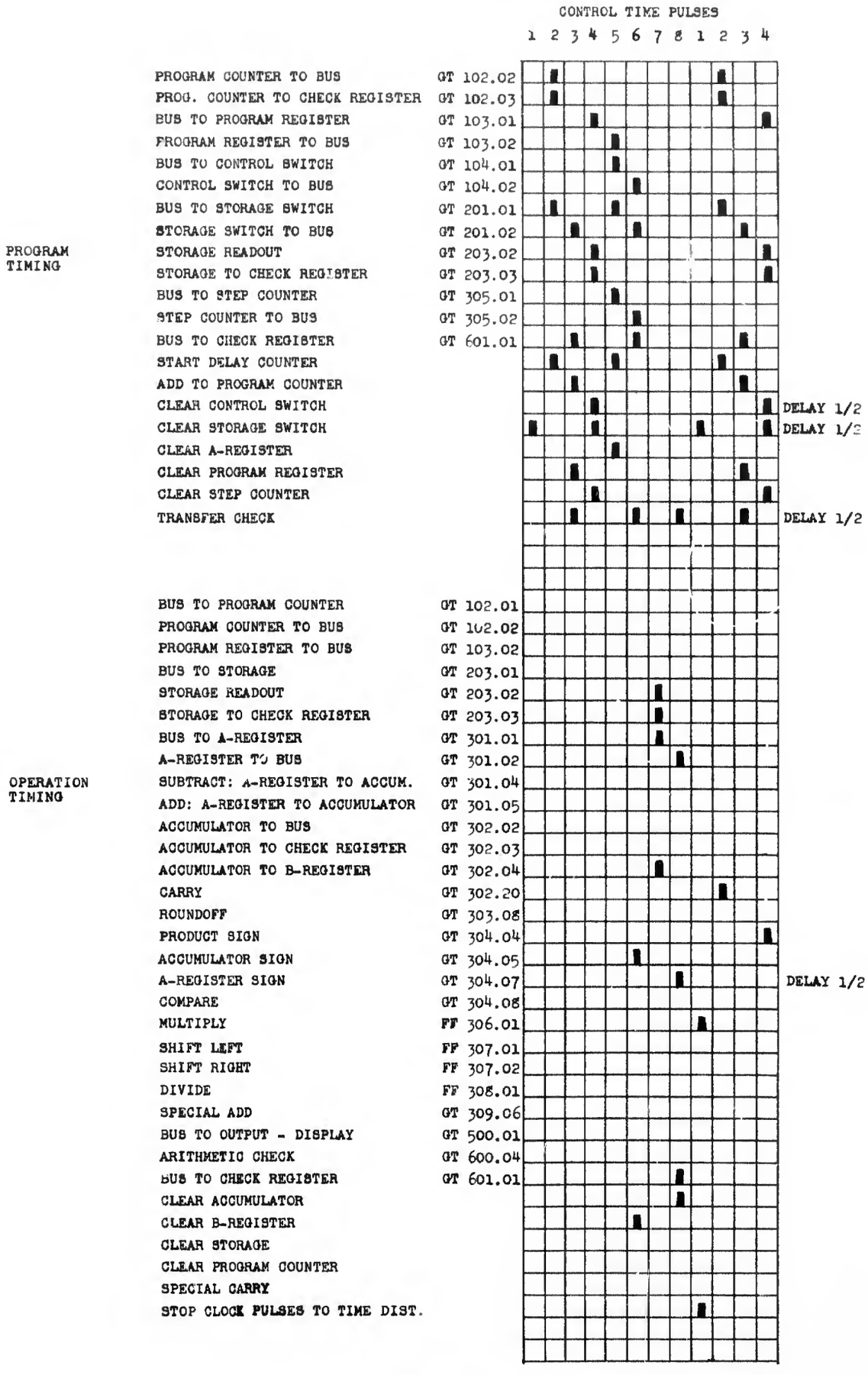

Figure 77

TIMING FOR MULTIPLY AND HOLD FULL PRODUCT

OPERATION: DIVIDE dv

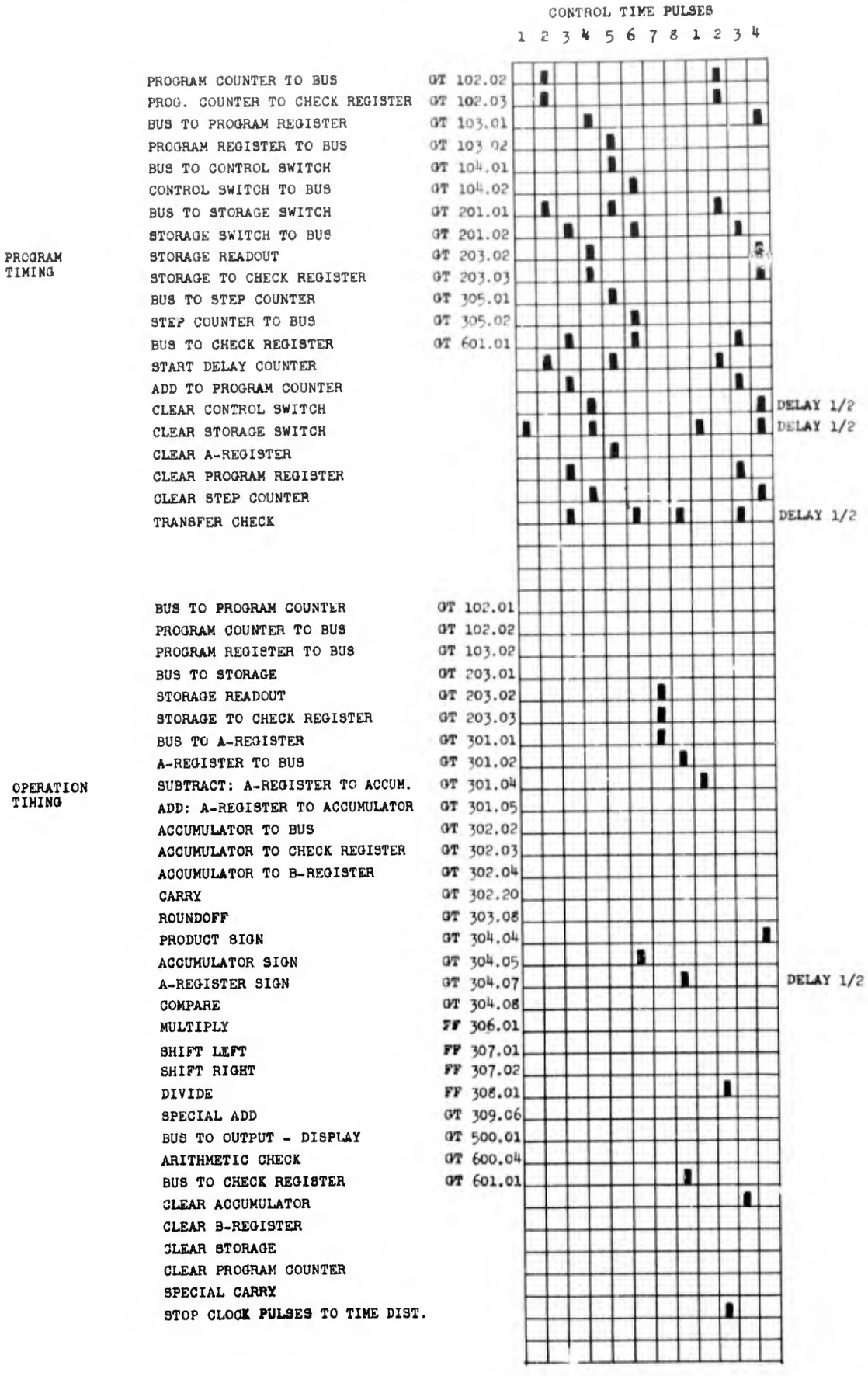

Figure 78

TIMING FOR DIVIDE

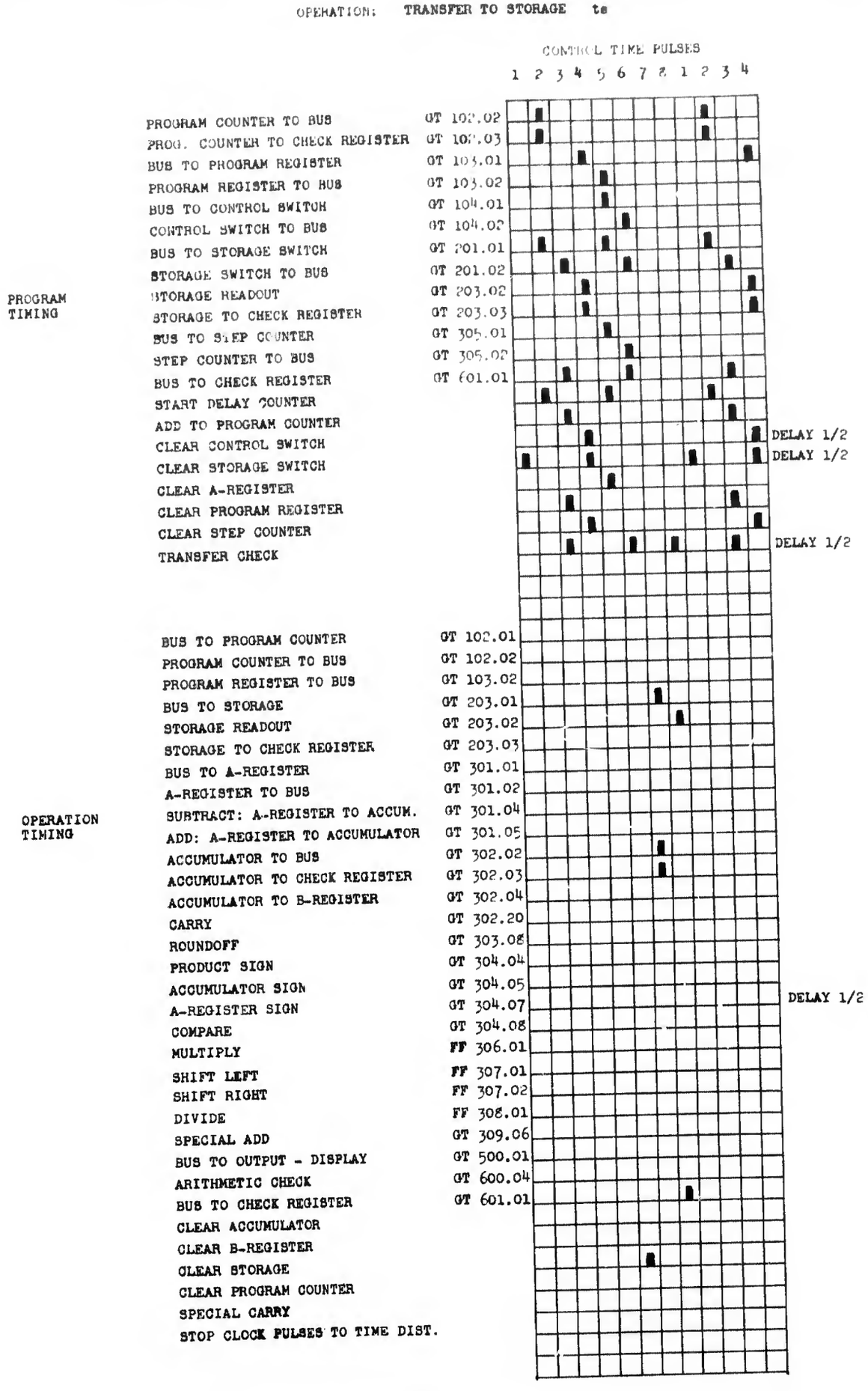

Figure 79

TIMING FOR TRANSFER TO STORAGE

OPERATION: SHIFT RIGHT sr

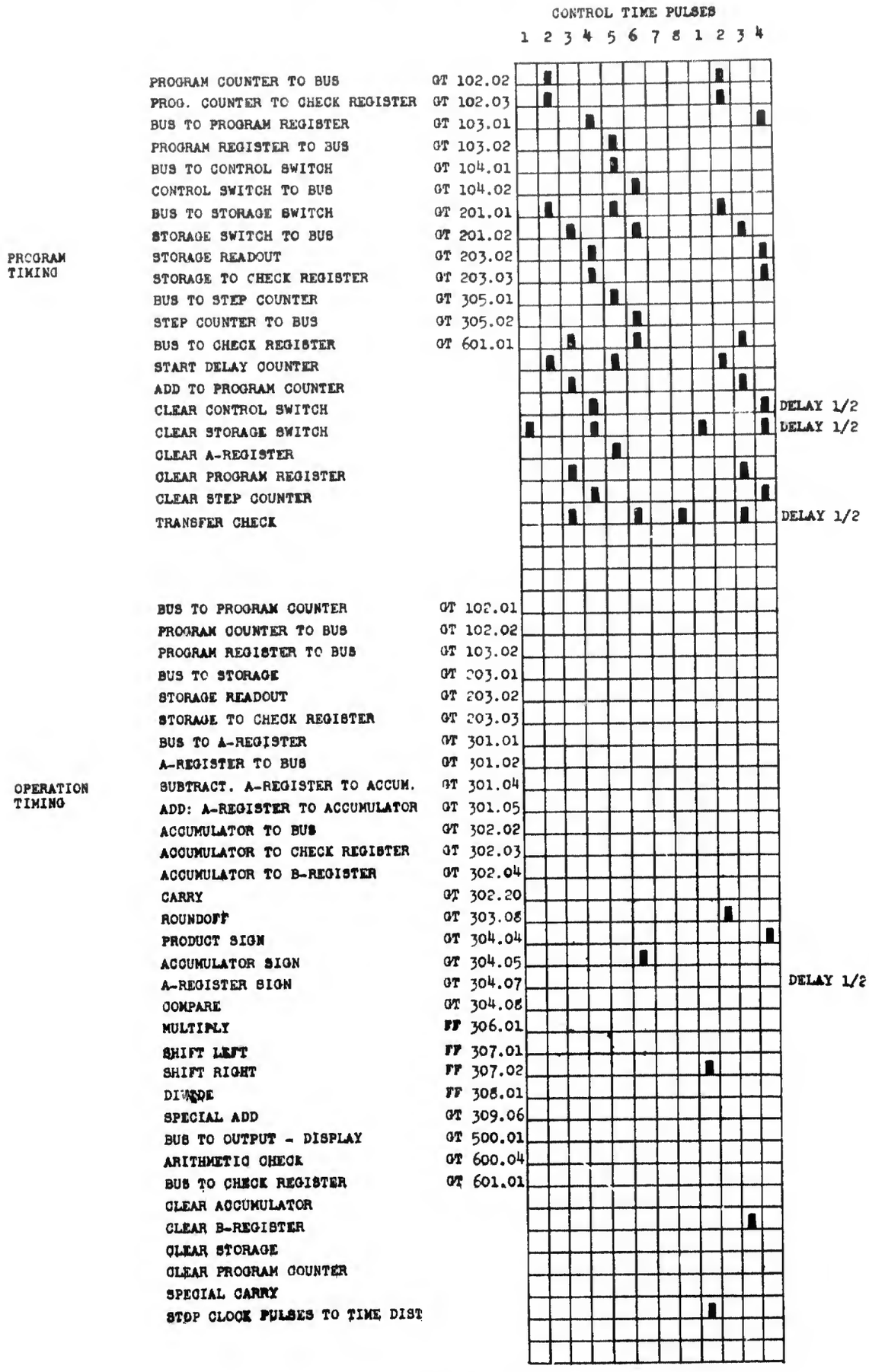

Figure 80

TIMING FOR SHIFT RIGHT

OPERATION: SHIFT LEFT s1

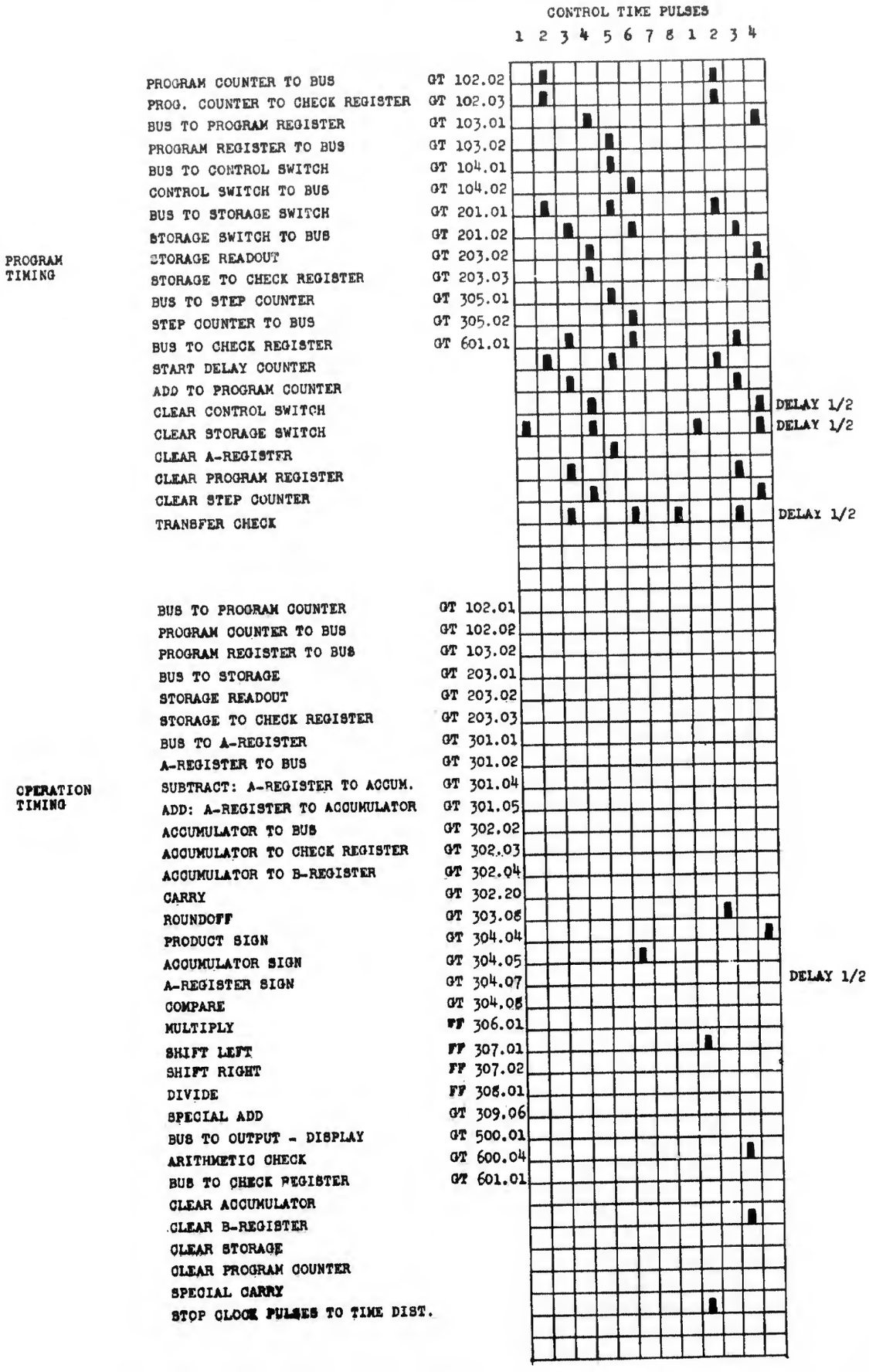

Figure 81

TIMING FOR SHIFT LEFT

OPERATION: SUBPROGRAM sp

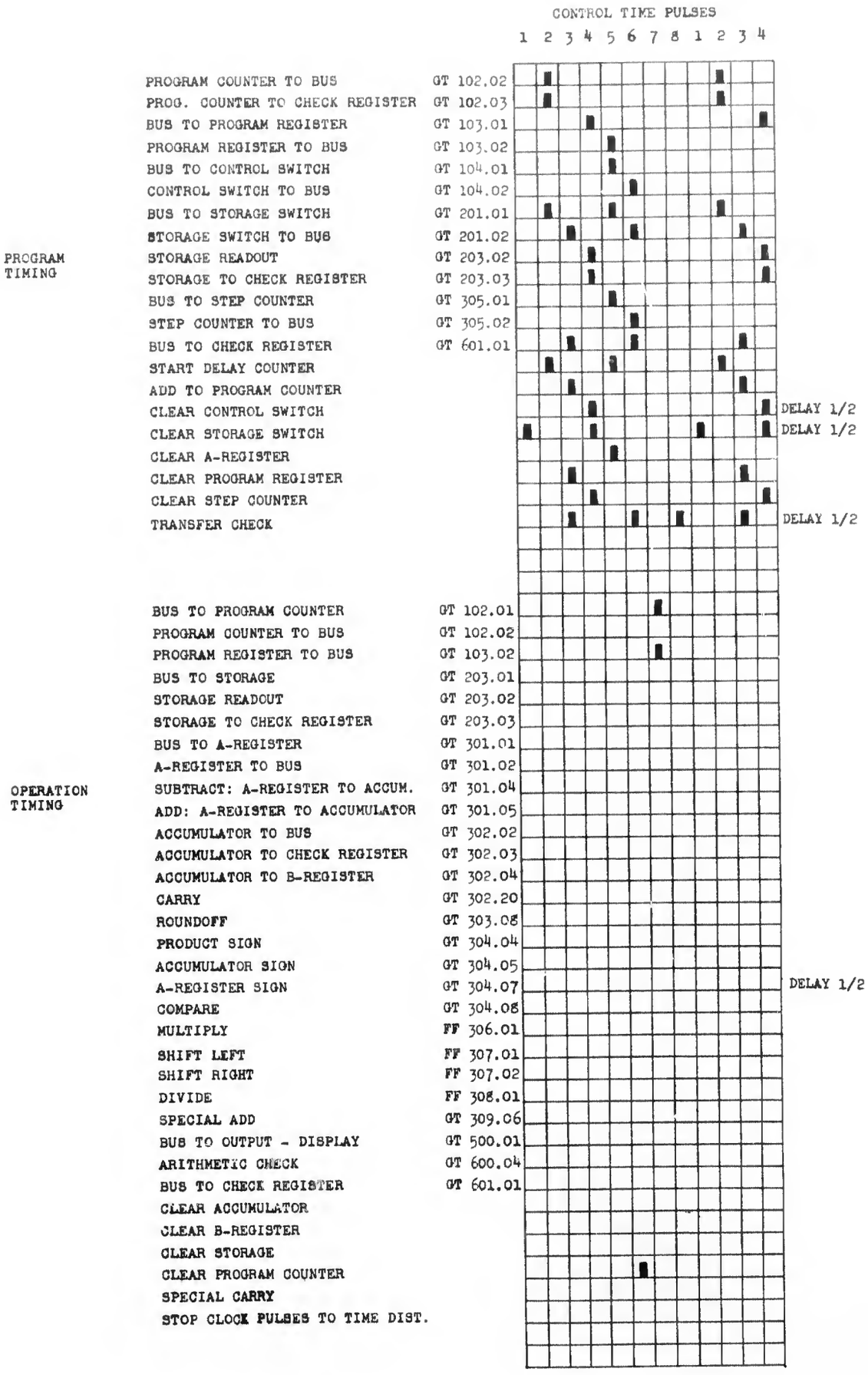

Figure 82

TIMING FOR SUBPROGRAM

OPERATION: COMPARE op

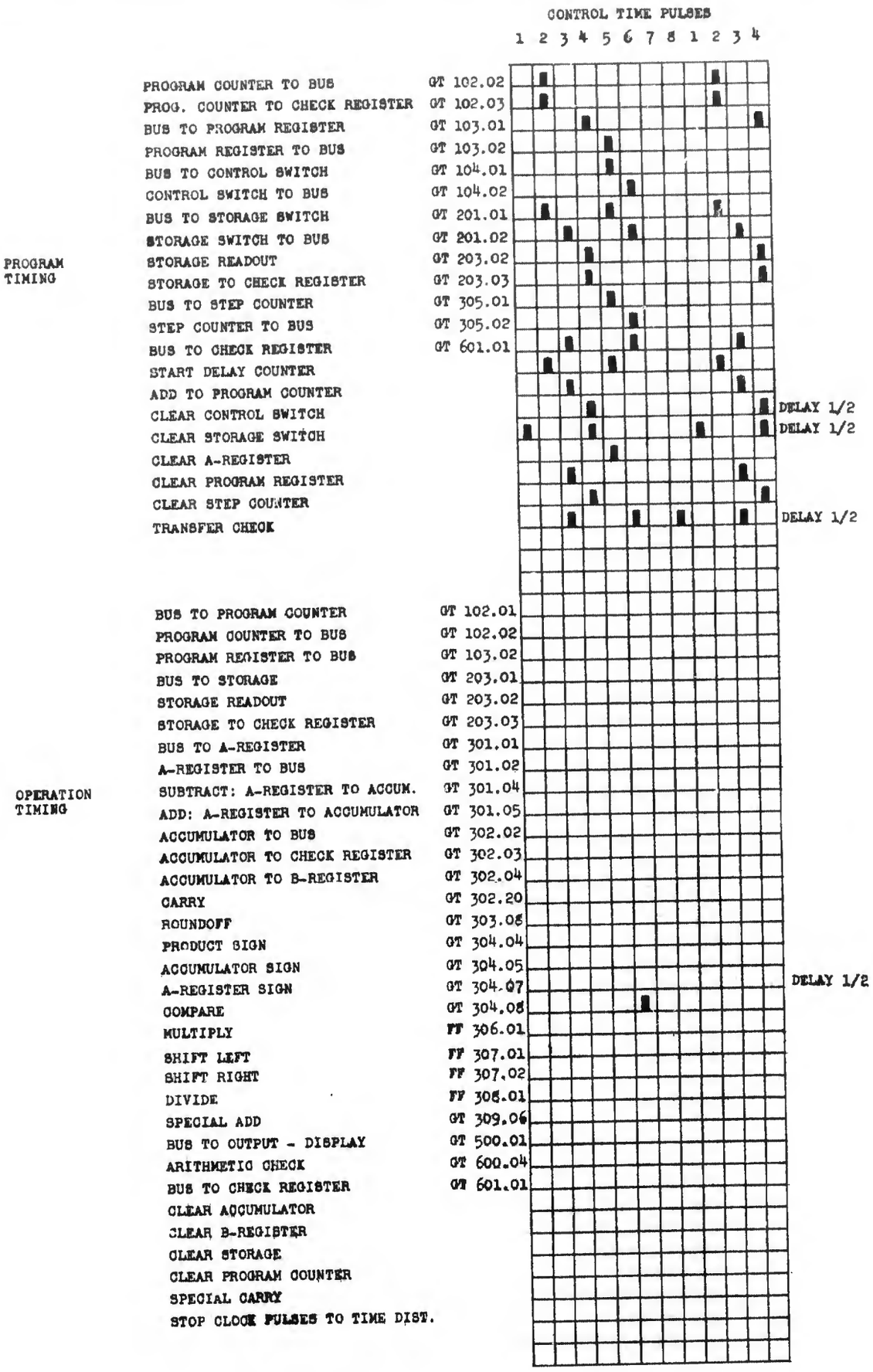

Figure 83

TIMING FOR CONDITIONAL PROGRAM

OPERATION: TRANSFER DIGITS td

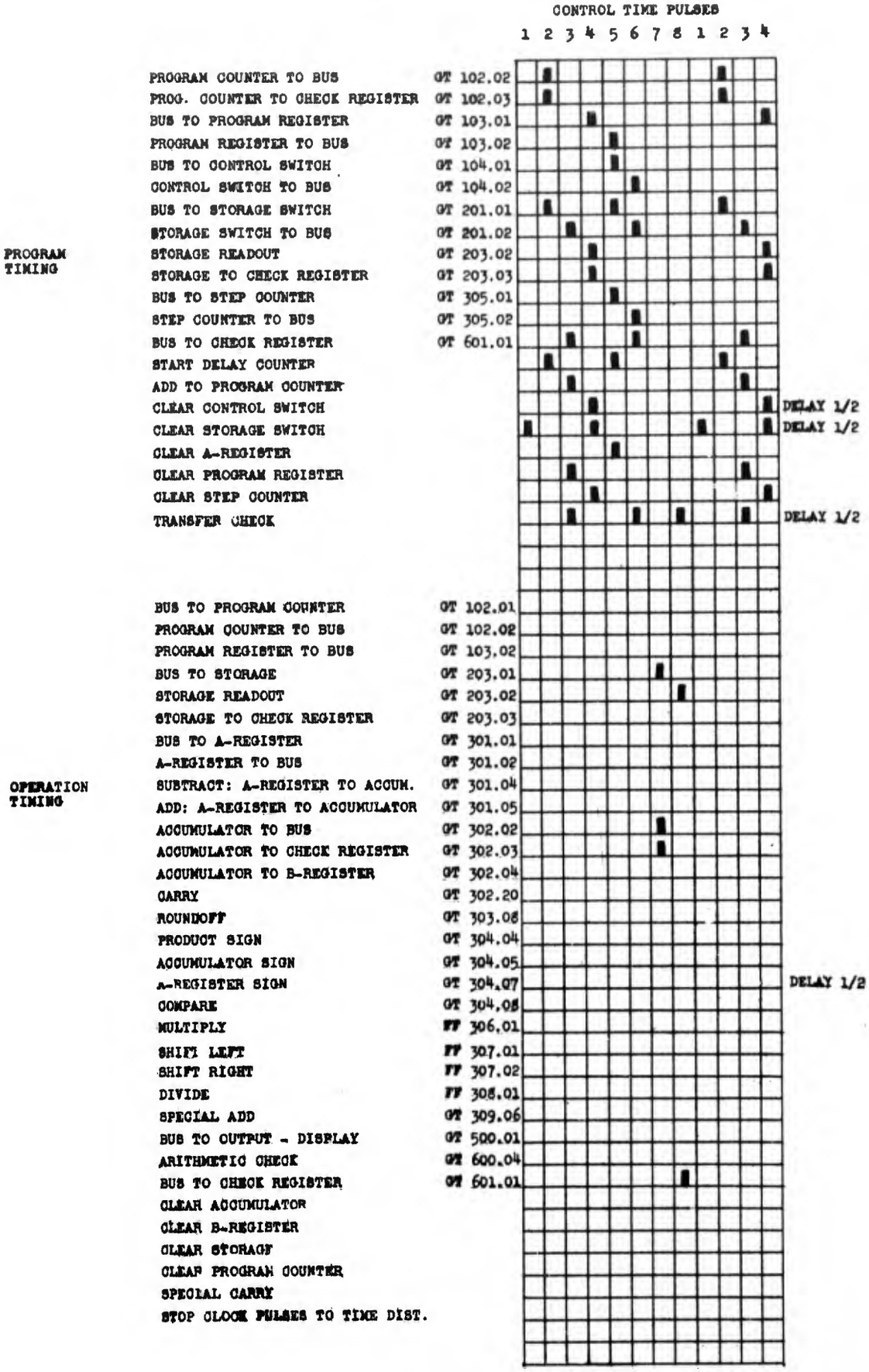

Figure 84

TIMING FOR TRANSFER DIGITS

OPERATION: SPECIAL ADD ss

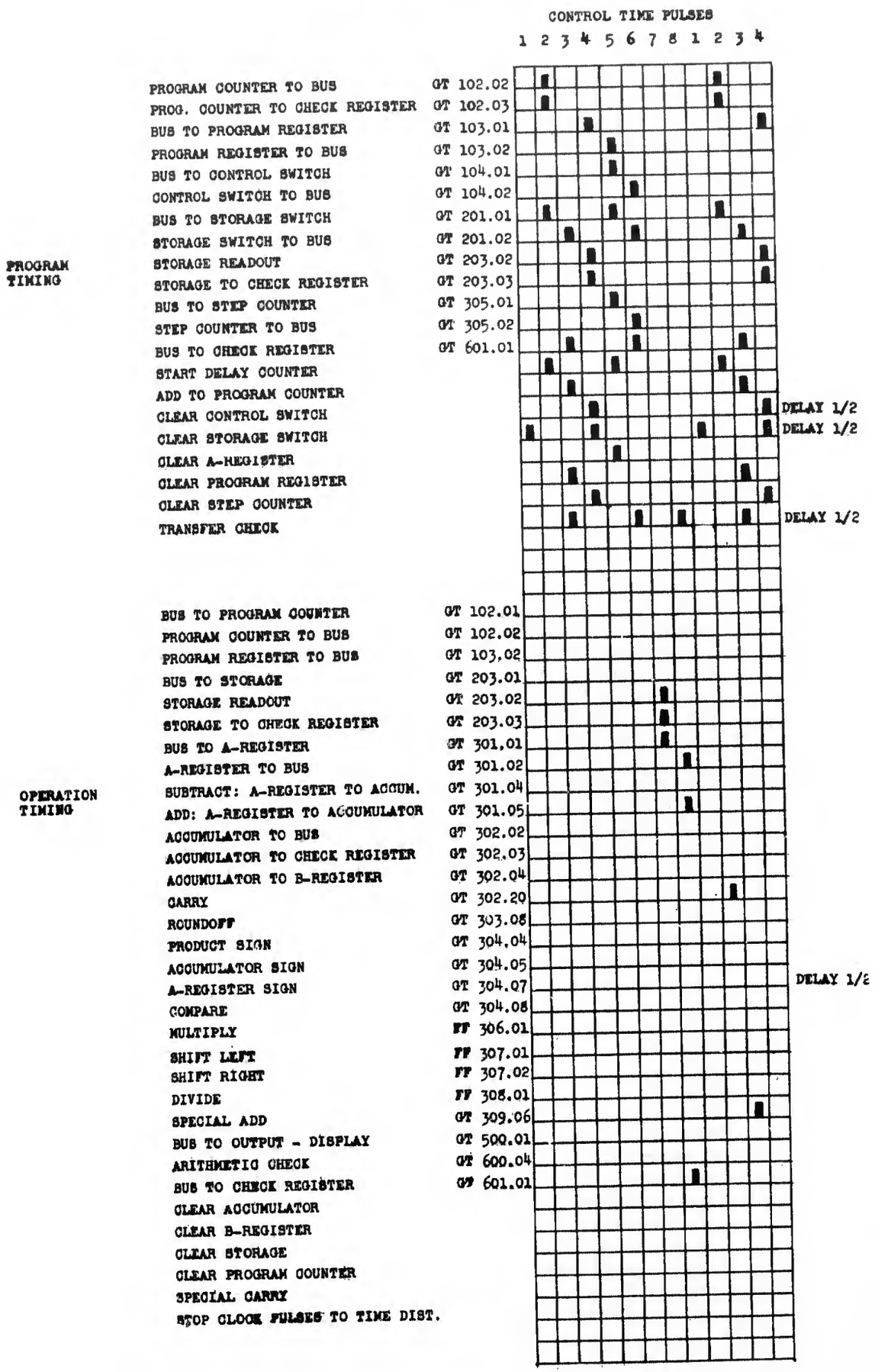

Figure 85

TIMING FOR SPECIAL ADD

OPERATION: STORE AND DISPLAY sd

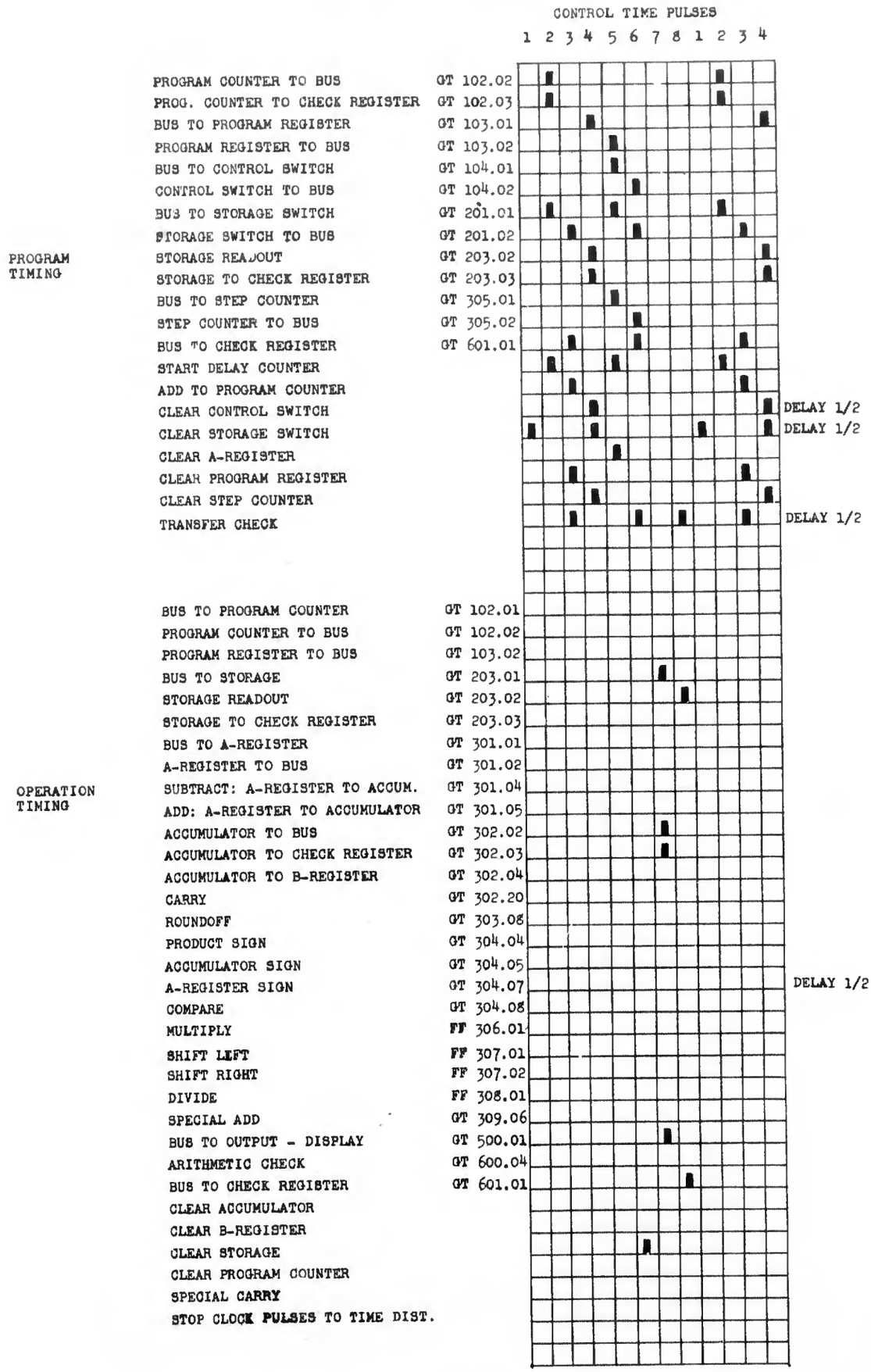

Figure 86

TIMING FOR STORE AND DISPLAY

UNIT CODE NUMBERS

100 Control

- 101 Master Clock
- 102 Program Counter
- 103 Program Register
- 104 Control Switch
- 105 Operation Matrix
- 106 Time Pulse Distributor
- 107 Operation Timing Matrix
- 108 Program Timing Matrix
- 109 Repeat Switch - (Removed from System)

200 Storage

- 201 Switch
- 202 Toggle Switch Storage
- 203 Flip Flop Stroage

300 Arithmetic Element

- 301 A-Register
- 302 Accumulator
- 303 B-Register
- 304 Sign Control
- 305 Step Counter
- 306 Multiply
- 307 Shift
- 308 Divide

400 Input

500 Output

600 Checking

- 601 Check Register

LETTER SYMBOLS

AC	Accumulator
BA	Buffer Amplifier
BC	Binary Coder
BD	Bus Driver
DE	Delay Element
ES	Electronic Switch
FD	Frequency Divider
FF	Flip Flop
GT	Gate Tube Circuit
IC	Intensity Control Circuit
PF	Pulse Forming Circuit
ST	Storage Tube
TG	Trigger Pulse Generator
TP	Timing Pulse Generator
TT	Trigger Tube

DRAWING SYMBOLS

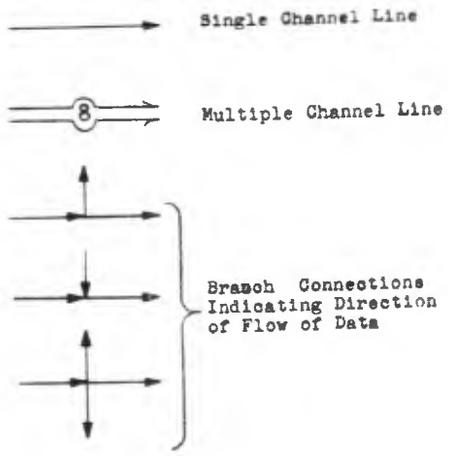

Figure 87

PARALLEL DIGIT COMPUTER CODES